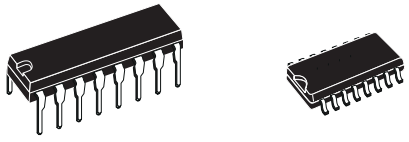
HCF40192B

PRESETTABLE UP/DOWN COUNTER (DUAL CLOCK WITH RESET) BCD TYPE

- INDIVIDUAL CLOCK LINES FOR COUNTING UP OR COUNTING DOWN
- SYNCHRONOUS HIGH-SPEED CARRY AND BORROW PROPAGATION DELAYS FOR CASCADING
- ASYNCHRONOUS RESET AND PRESET CAPABILITY
- MEDIUM-SPEED OPERATION - f_{CL} = 8MHz (typ.) AT 10 V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP SOP

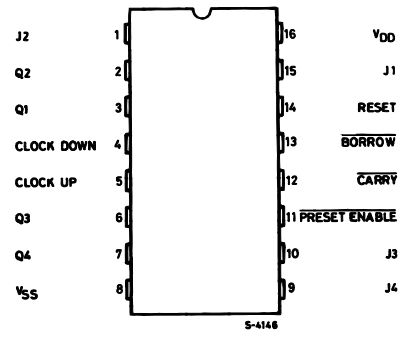
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF40192BEY	
SOP	HCF40192BM1	HCF40192M013TR

DESCRIPTION

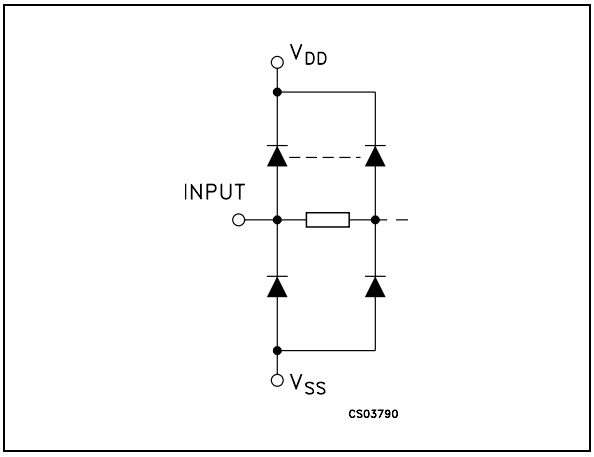
HCF40192B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
HCF40192B Presettable BCD Up/Down Counter consists of 4 synchronously clocked, GATED "D" type flip-flops connected as a counter. The inputs consist of four individual jam lines, a PRESET ENABLE control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs, as well as CARRY and BORROW outputs for multiple-stage counting schemes, are provided. The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the PRESET ENABLE control is low. The counter counts up one count on the positive clock edge of the CLOCK UP signal, provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high. The CARRY and BORROW signals are high when the counter is counts up or down. The CARRY signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The BORROW signal goes

PIN CONNECTION



low one-half clock cycle after the counter reaches its minimum count in the count-down mode. The cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the $\overline{\text{BORROW}}$ and $\overline{\text{CARRY}}$ outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the following package.

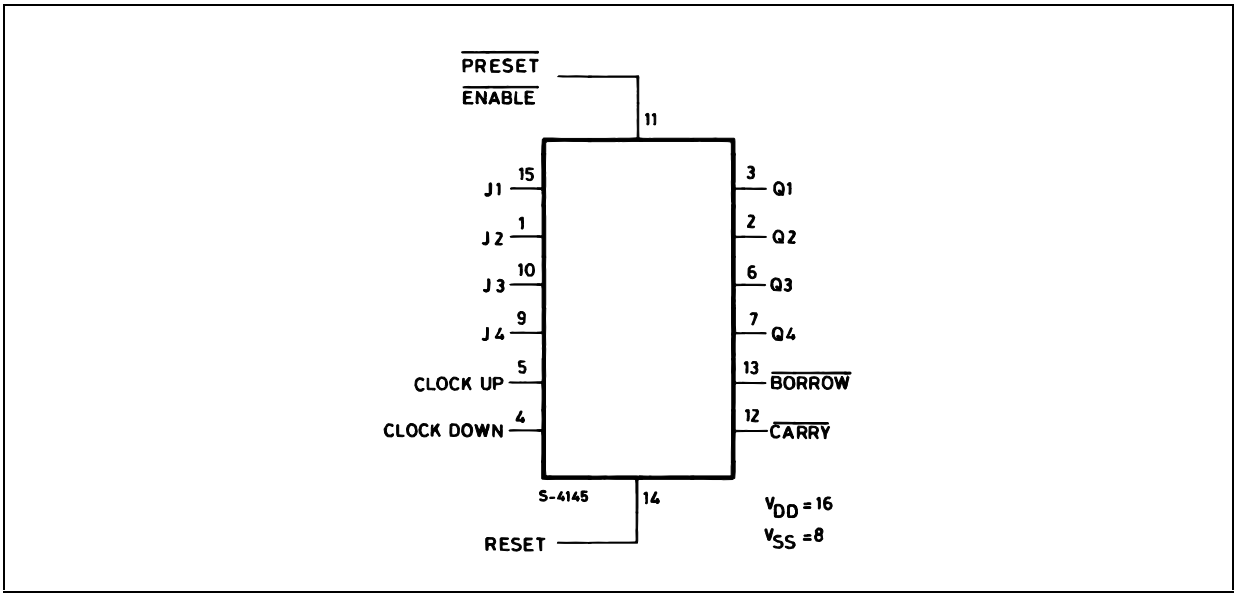
IINPUT EQUIVALENT CIRCUIT



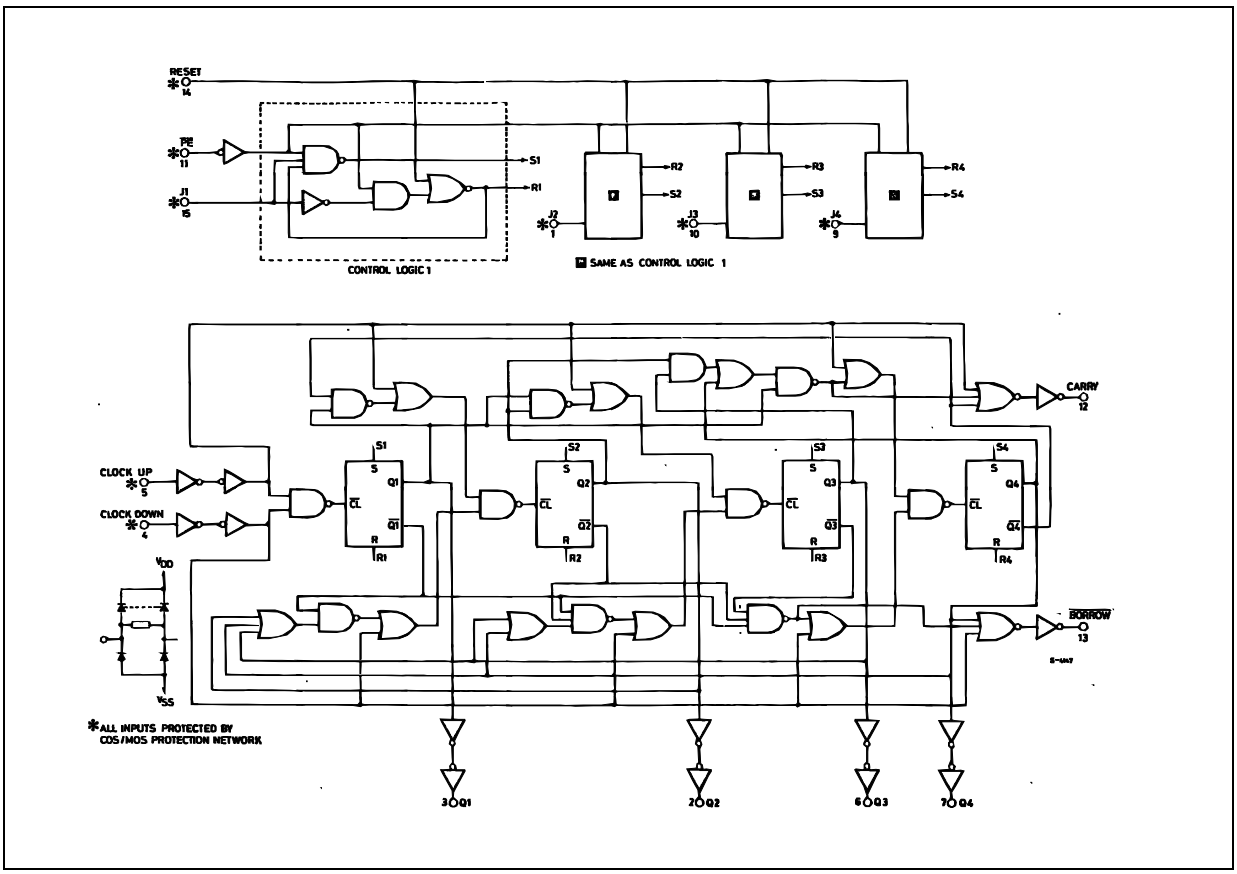
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q1 to Q4	Flip-Flop Outputs
4	CLOCK DOWN	Clock Down Input
5	CLOCK UP	Clock Up Input
11	$\overline{\text{PRESET ENABLE}}$	Preset Enable Input
12	$\overline{\text{CARRY}}$	Count Up (Carry)
13	$\overline{\text{BORROW}}$	Count Down (Borrow)
14	RESET	Reset Input
15, 1, 10, 9	J1 to J4	Data Input
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



LOGIC DIAGRAM

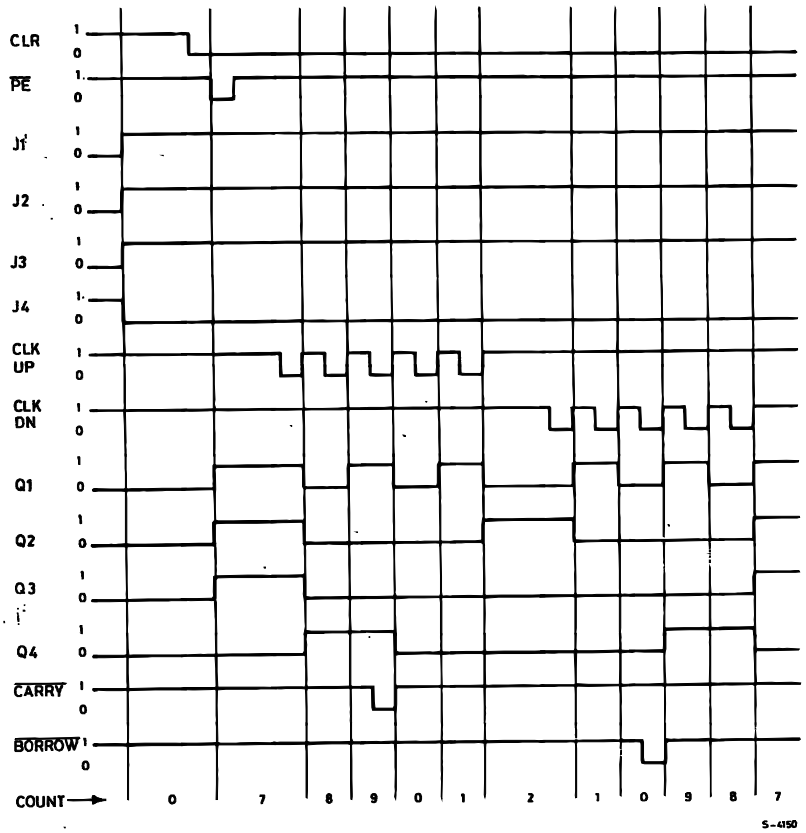


TRUTH TABLE

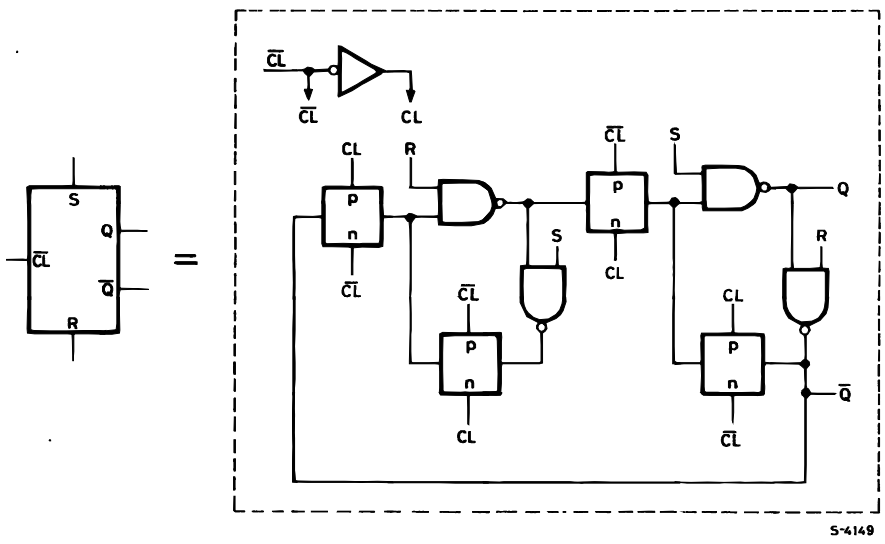
CLOCK UP	CLOCK DOWN	$\overline{\text{PRESET ENABLE}}$	RESET	ACTION
⌐¯	H	H	L	COUNT UP
¯⌐	H	H	L	NO COUNT
H	⌐¯	H	L	COUNT DOWN
H	¯⌐	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

(X) : Don't Care

TIMING DIAGRAM



INTERNAL LOGIC FLIP-FLOP



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

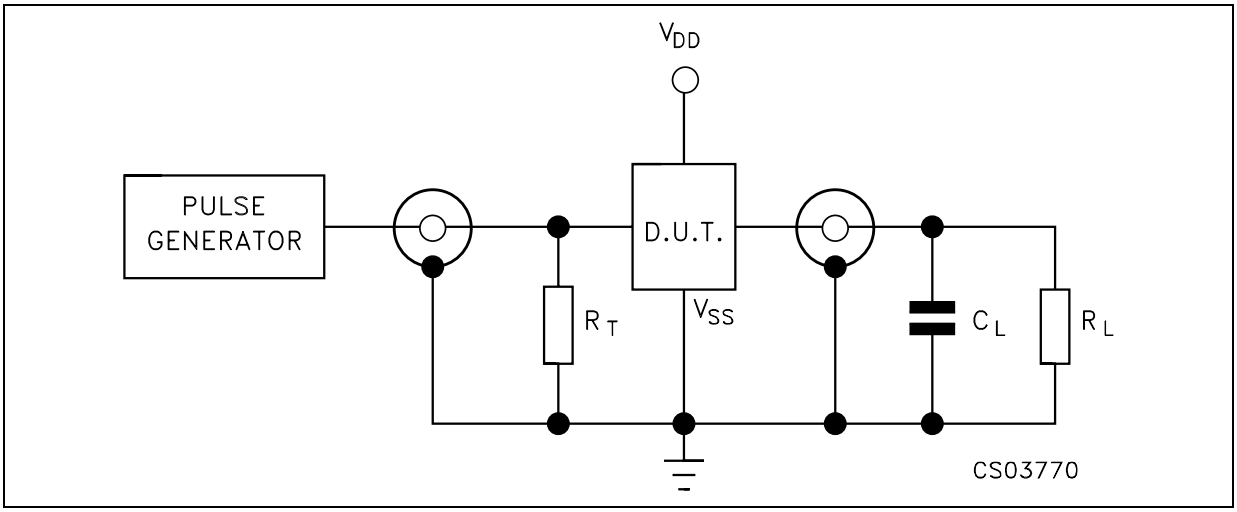
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time Clock Up or Clock Down to Q Reset to Q	5			250	500	ns
		10			120	240	
		15			90	180	
	$\overline{PE}$ to Q	5			200	400	ns
		10			100	200	
		15			70	140	
	Clock Up to $\overline{Carry}$ Clock Down to $\overline{Borrow}$	5			160	320	ns
		10			80	160	
		15			60	120	
	$\overline{Reset}$ or $\overline{PR}$ to $\overline{Borrow}$ or $\overline{Carry}$	5			300	600	ns
		10			150	300	
		15			110	220	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{rem}*	Removal Time Reset or $\overline{PE}$	5		80	40		ns
		10		40	20		
		15		30	15		
t_W	Clock Input Pulse Width Reset	5		480	240		ns
		10		300	150		
		15		260	130		
	$\overline{PE}$	5			120	240	ns
		10			85	170	
		15			70	140	
	Clock	5			90	180	ns
		10			45	90	
		15			30	60	
t_r t_f	Clock Input Rise or Fall Time	5				15	µs
		10				15	
		15				5	
f_{CL}	Maximum Clock Input Frequency	5		2	4		MHz
		10		5	8		
		15		5.5	11		

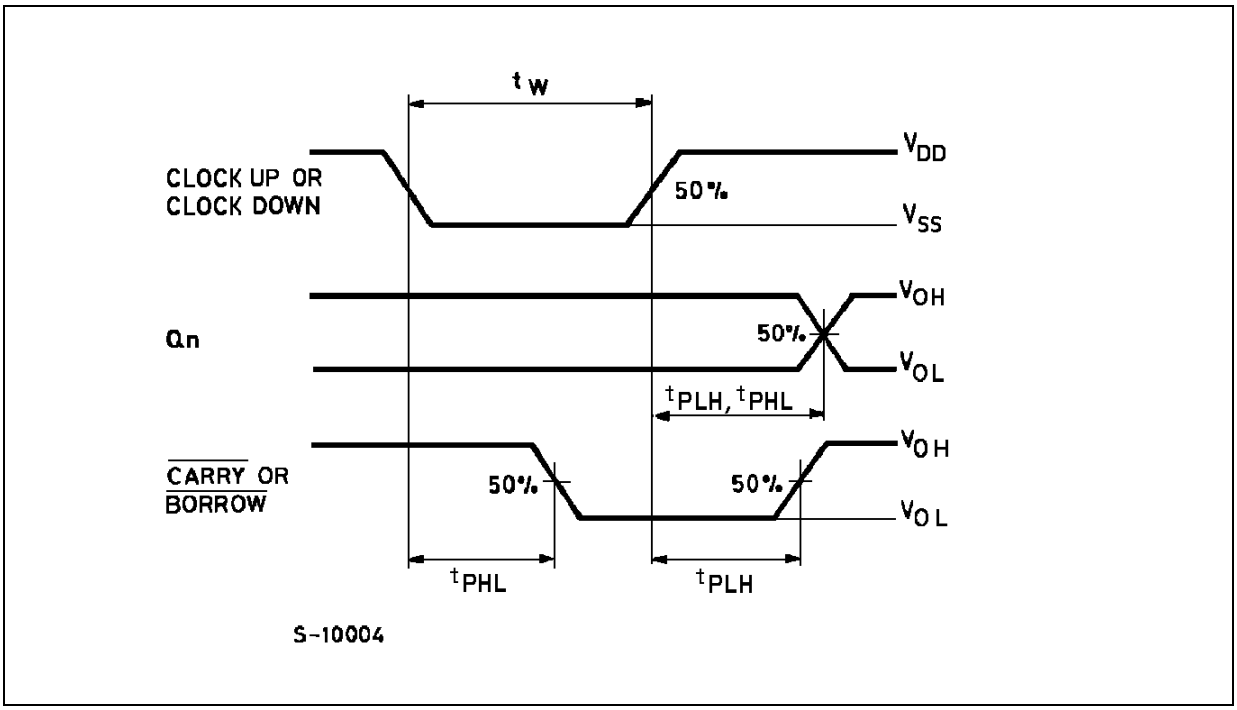
(*) The time required for Reset or Preset Enable control to be removed before clocking (see timing diagram).

TEST CIRCUIT

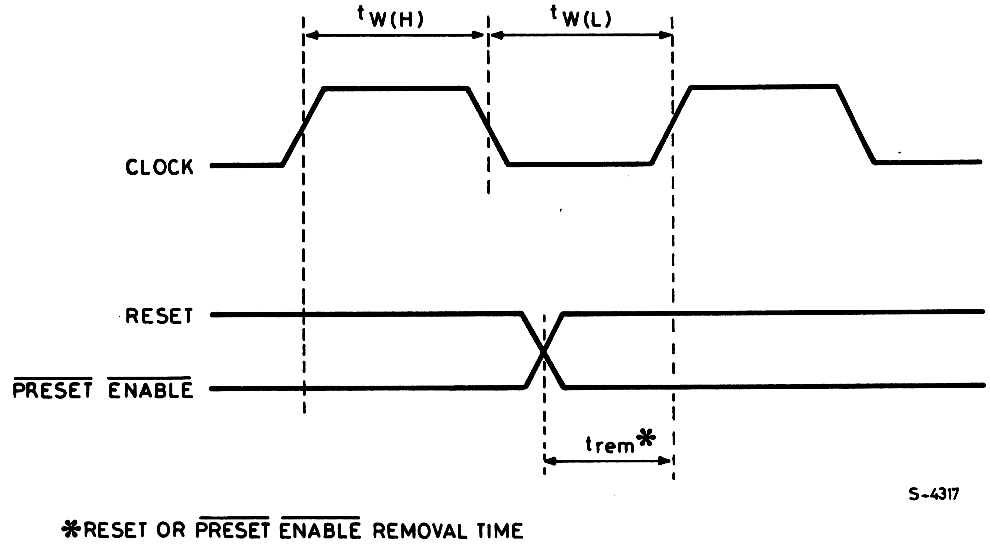


C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

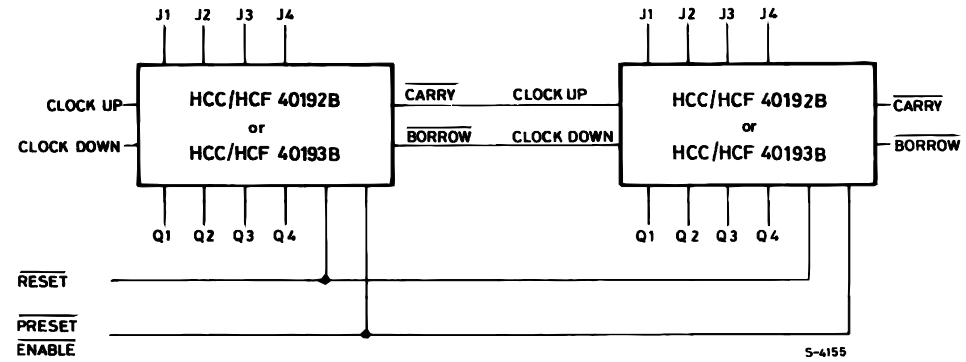
WAVEFORM 1 : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2 : MINIMUM PULSE WIDTH AND REMOVAL TIME (f=1MHz; 50% duty cycle)

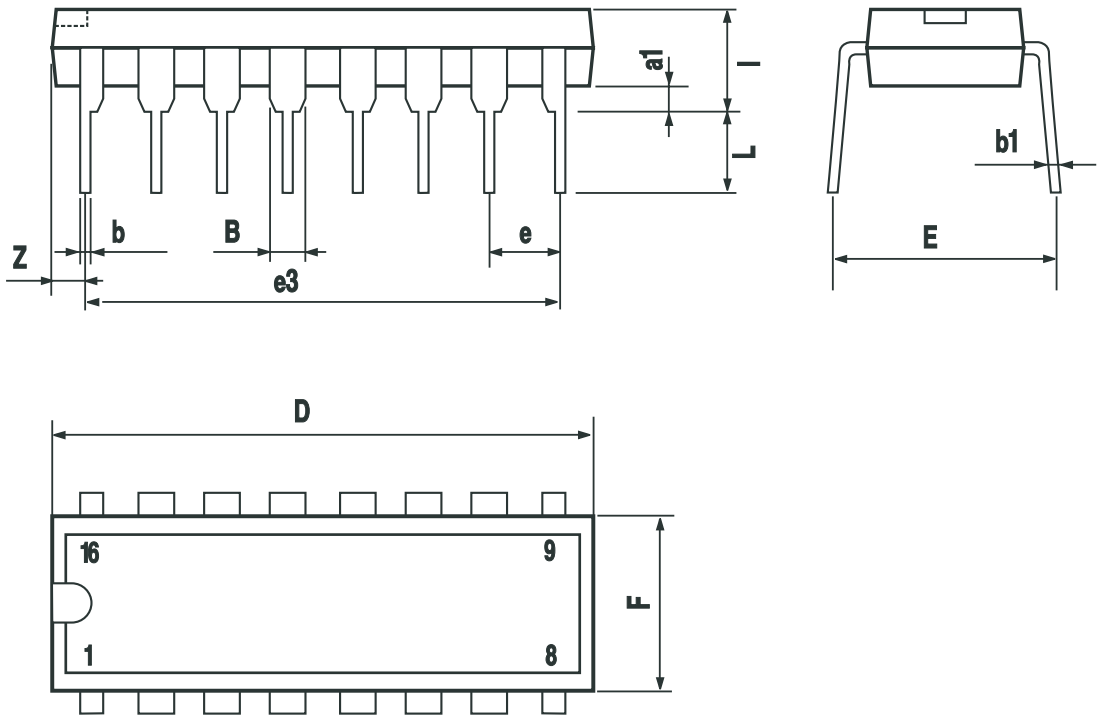


TYPICAL APPLICATION: CASCADED COUNTER PACKAGES



Plastic DIP-16 (0.25) MECHANICAL DATA

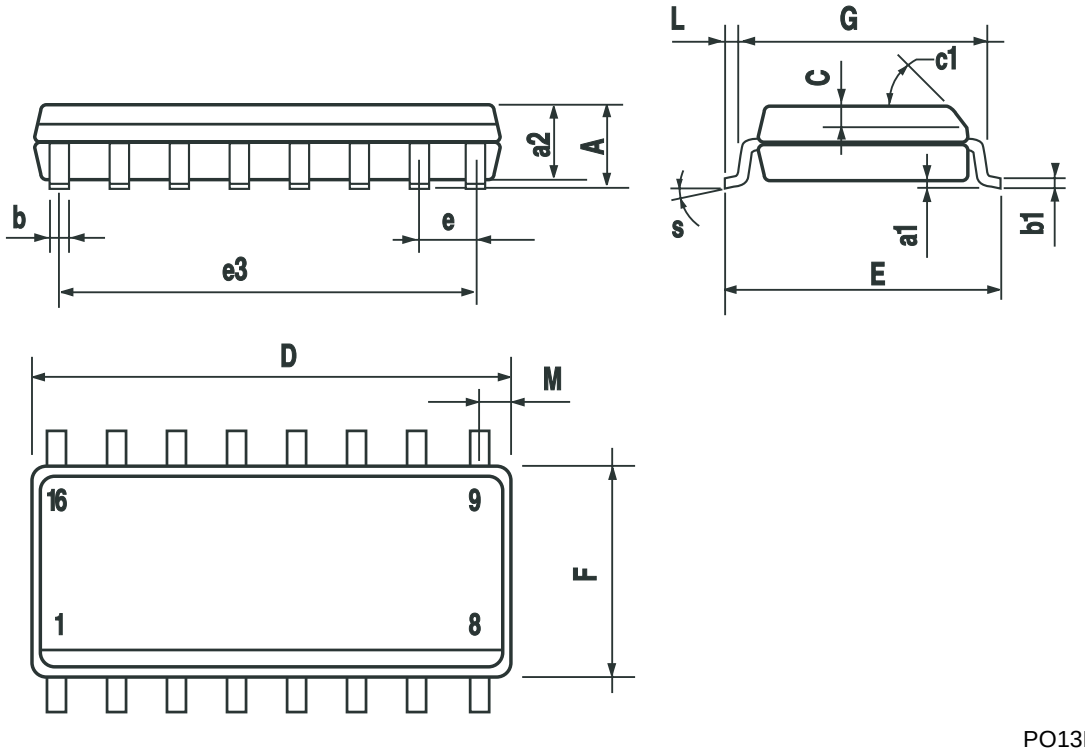
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H