MOTOROLA

MC14551B

CMOS MSI

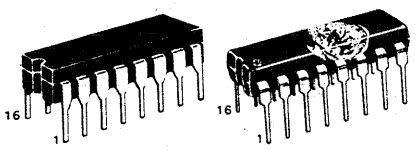
(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT ANALOG MULTIPLEXER/ DEMULTIPLEXER

QUAD 2-INPUT ANALOG MULTIPLEXER/DEMULTIPLEXER

The MC14551B is a digitally controlled analog switch. It is an effective 4 PDT switch with low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

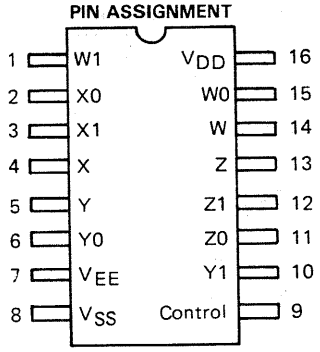
- High On/Off Output Ratio — 65 dB typical
- Quiescent Current = 5.0 nA/Package typical at 5 Vdc
- Low Crosstalk Between Switches — 80 dB typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (V_{DD}-V_{EE}) = 3 to 18 V
  Note: V_{EE} must be ≤ V_{SS}
- Transmits Frequencies Up To 65 MHz
- Linearized Transfer Characteristics, ΔR_{ON} < 60 Ω for V_{in} at V_{DD} to V_{EE} at 15 Vdc
- Low Noise — 12 n/V$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical



CASE 620
L SUFFIX
CERAMIC PACKAGE

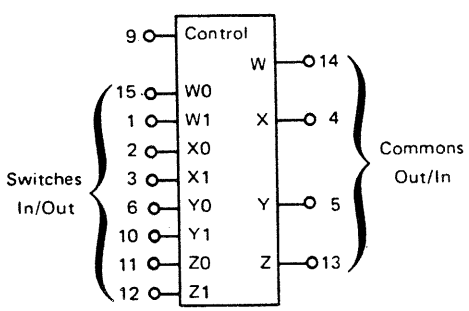
CASE 648
P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage V_{DD} – V_{EE}	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
Through Current	I	25	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Note: Control Input referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}.

ELECTRICAL CHARACTERISTICS ($V_{EE} = V_{SS}$)

Characteristic	Symbol	V_{DD}	T_{low}*		25°C			T_{high}*		Unit
		Vdc	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (Control) "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	—	11.0	8.25	—	11.0	—	
Input Current (Control) (AL Device)	I_{in}	15	—	±0.1	—	± 0.00001	±0.1	—	±1.0	µAdc
Input Current (Control) (CL/CP Device)	I_{in}	15	—	±0.3	—	± 0.00001	±0.3	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}									pF
Control, Inhibit		—	—	—	—	5.0	7.5	—	—	
Switch Inputs (Inhibit = 1)		—	—	—	—	10	21.0	—	—	
Output Capacitance	C_{out}	10	—	—	—	17	—	—	—	pf
Feedthrough Capacitance	C_{in-out}	10	—	—	—	0.10	—	—	—	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	—	20	—	0.005	20	—	150	µAdc
		10	—	40	—	0.010	40	—	300	
		15	—	80	—	0.015	80	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package)	I_T	5.0	$I_T = (0.07\ \mu A/kHz)\ f + I_Q$							µAdc
		10	$I_T = (0.20\ \mu A/kHz)\ f + I_Q$							
		15	$I_T = (0.36\ \mu A/kHz)\ f + I_Q$							
On Resistance (AL Device)	R_{ON}	5.0	—	800	—	250	1050	—	1300	Ω
		10	—	400	—	120	500	—	550	
		15	—	220	—	80	280	—	320	
On Resistance (CL/CP Device)	R_{ON}	5.0	—	880	—	250	1050	—	1200	Ω
		10	—	450	—	120	500	—	520	
		15	—	250	—	80	280	—	300	
Δ ON resistance Between Any Two Channels	ΔR_{ON}	5.0	—	—	—	25	—	—	—	Ω
		10	—	—	—	10	—	—	—	
		15	—	—	—	5.0	—	—	—	
OFF Channel Leakage Current	—									nAdc
(AL Device)		15	—	±100	—	±0.01	±100	—		
Any Channel									±1000	
All Channels OFF:		15	—	±100	—	±0.02	±100	—	±1000	
OFF Channel Leakage Current	—									nAdc
(CL/CP Device)		15	—	±300	—	±0.01	±300	—		
Any Channel									±1000	
All Channels OFF:		15	—	±300	—	±0.02	±300	—	±1000	

* T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
Noise immunity is defined as the control input voltage coincident with the specified change, ΔV_{out}, at an output in the OFF State.

** The formulae given are for the typical characteristics only at 25°C.

† Total Supply Current, I_T, is the current drawn at device terminals V_{DD} and V_{SS} for total current through the device. The channel component $(V_{in}-V_{out})/R_{ON}$, should not be included.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}-V_{SS} Vdc	Min	Typ	Max	Unit
Propagation Delay Times Switch Input to Switch Output (R_L = 10kΩ)	t_{PLH},t_{PHL}					ns
t_{PLH},t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	–	35	90	
t_{PLH},t_{PHL} = (0.08 ns/pF) C_L + 11 ns		10	–	15	40	
t_{PLH},t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	–	12	30	
Inhibit to Output (R_L = 10 kΩ): Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level	t_{PHZ},t_{PLZ} t_{PZH},t_{PZL}					ns
		5.0	–	360	900	
		10	–	160	375	
		15	–	120	300	
Control Input to Output (R_L = 10 kΩ)	t_{PLH},t_{PHL}					ns
		5.0	–	350	875	
		10	–	140	350	
		15	–	100	250	
Sine Wave Distortion (R_L = 1 kΩ, f = 1 kHz)	–	10	–	0.04	–	%
Bandwidth (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} – V_{EE}) p-p, 20 $\text{Log}_{10}\frac{V_{out}}{V_{in}}$ = –3 dB)	BW	10	–	55	–	MHz
Feedthrough Attenuation, Input to Output (R_L = 1 kΩ, V_{in} = ½ (V_{DD}-V_{EE}) p-p, 20 $\text{Log}_{10}\frac{V_{out}}{V_{in}}$ = –50 dB)	–	10	–	3.0	–	MHz
Channel Separation (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} – V_{EE}) p-p, 20 $\text{Log}_{10}\frac{V_{out(B)}}{V_{in(A)}}$ = –50 dB)	–	10	–	3.0	–	MHz
Feedthrough Control, Input to Output (R1 = 1 kΩ, R_L = 10 kΩ, Control/Inhibit t_r = t_f = 20 ns	–	10	–	30	–	mV
Maximum Control Frequency (R_L = 1 kΩ, V_{out} = 1/2 V_{in})	–	10	–	10	–	MHz

*The formulas given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC

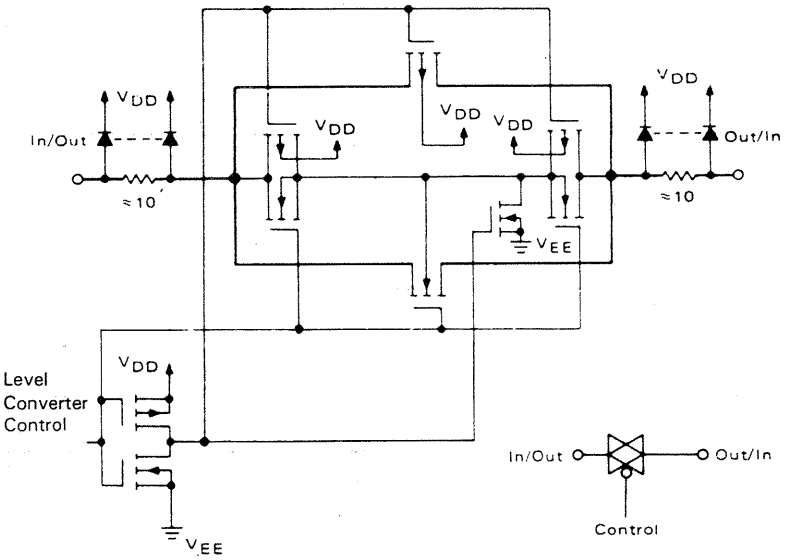
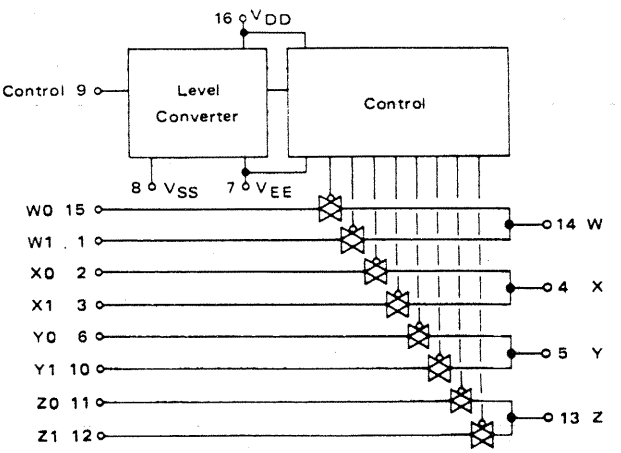


FIGURE 2 – MC14551B FUNCTIONAL DIAGRAM



TEST CIRCUITS

FIGURE 3 – INPUT VOLTAGE

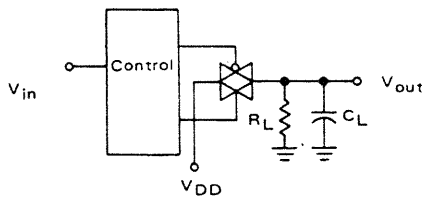


FIGURE 4 – PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

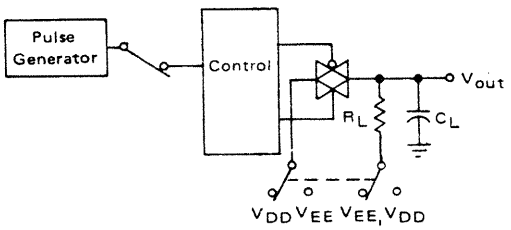


FIGURE 5 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

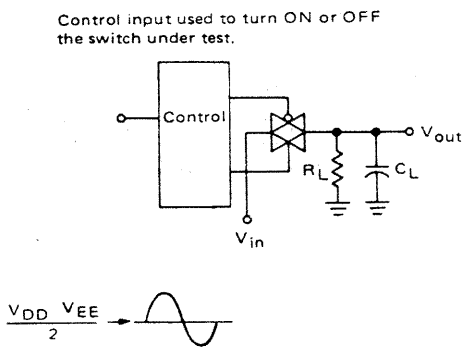


FIGURE 6 – CROSSTALK BETWEEN ANY TWO SWITCHES

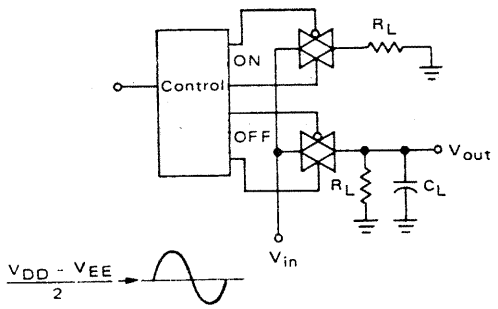


FIGURE 7 – FEEDTHROUGH, CONTROL TO SIGNAL OUTPUT

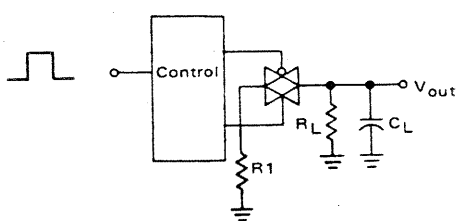


FIGURE 8 – MAXIMUM CONTROL FREQUENCY

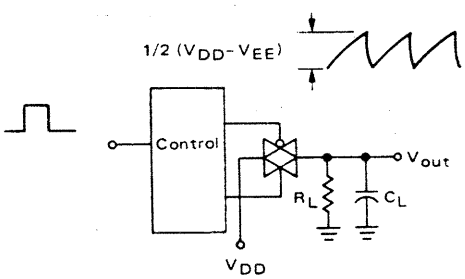
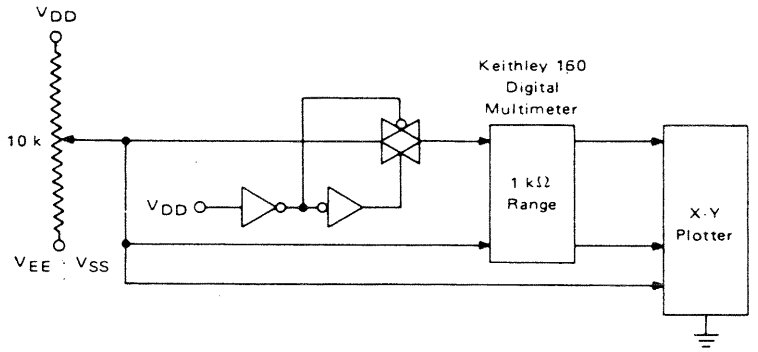


FIGURE 9 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 10 – V_{DD} @ 7.5 V, V_{EE} @ –7.5V

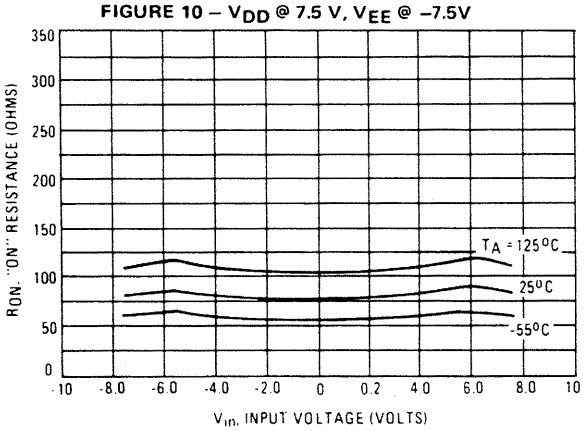


FIGURE 11 – V_{DD} @ 5.0V, V_{EE} @ –5.0 V

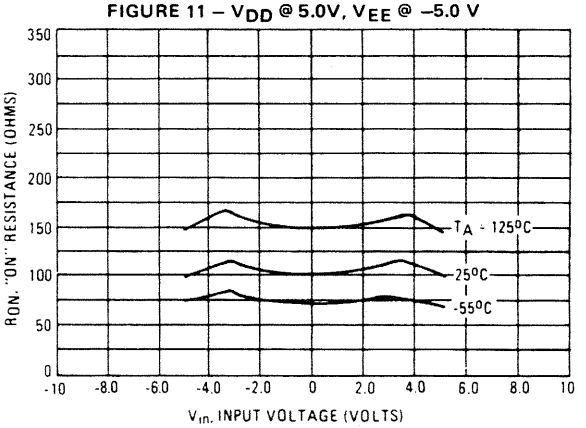


FIGURE 12 – V_{DD} @ 2.5 V, V_{EE} @ –2.5 V

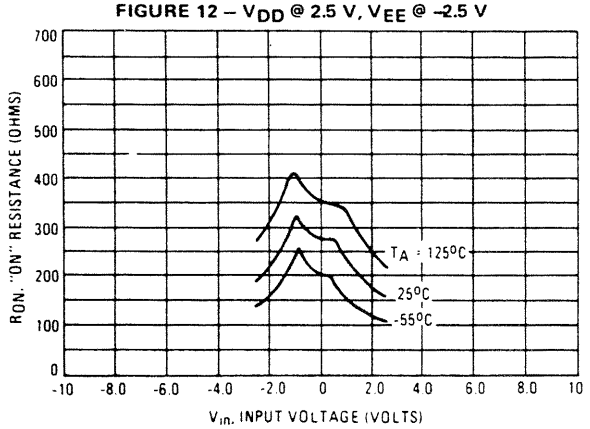


FIGURE 13 – COMPARISON at 25°C, V_{DD} @ $-V_{EE}$