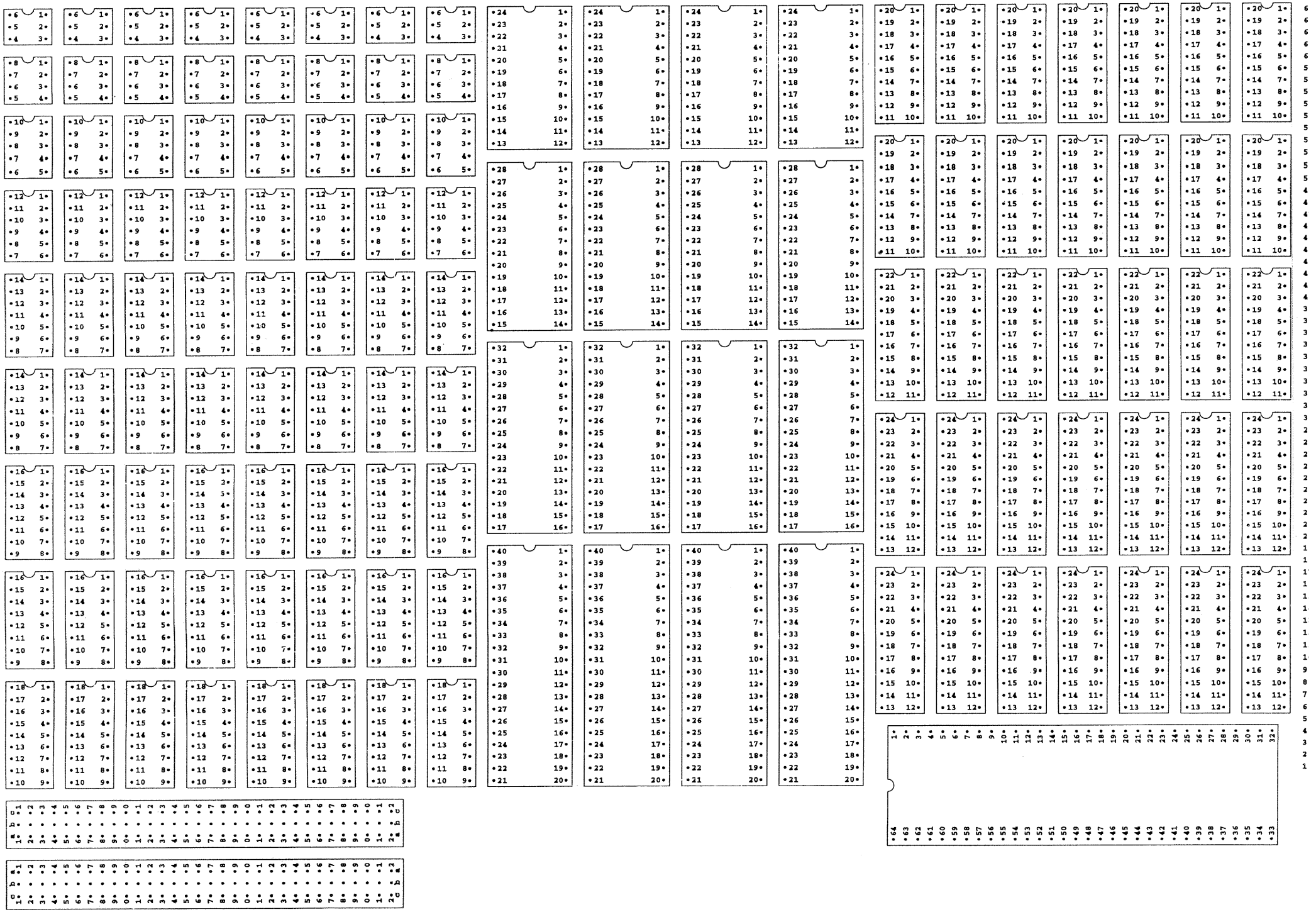
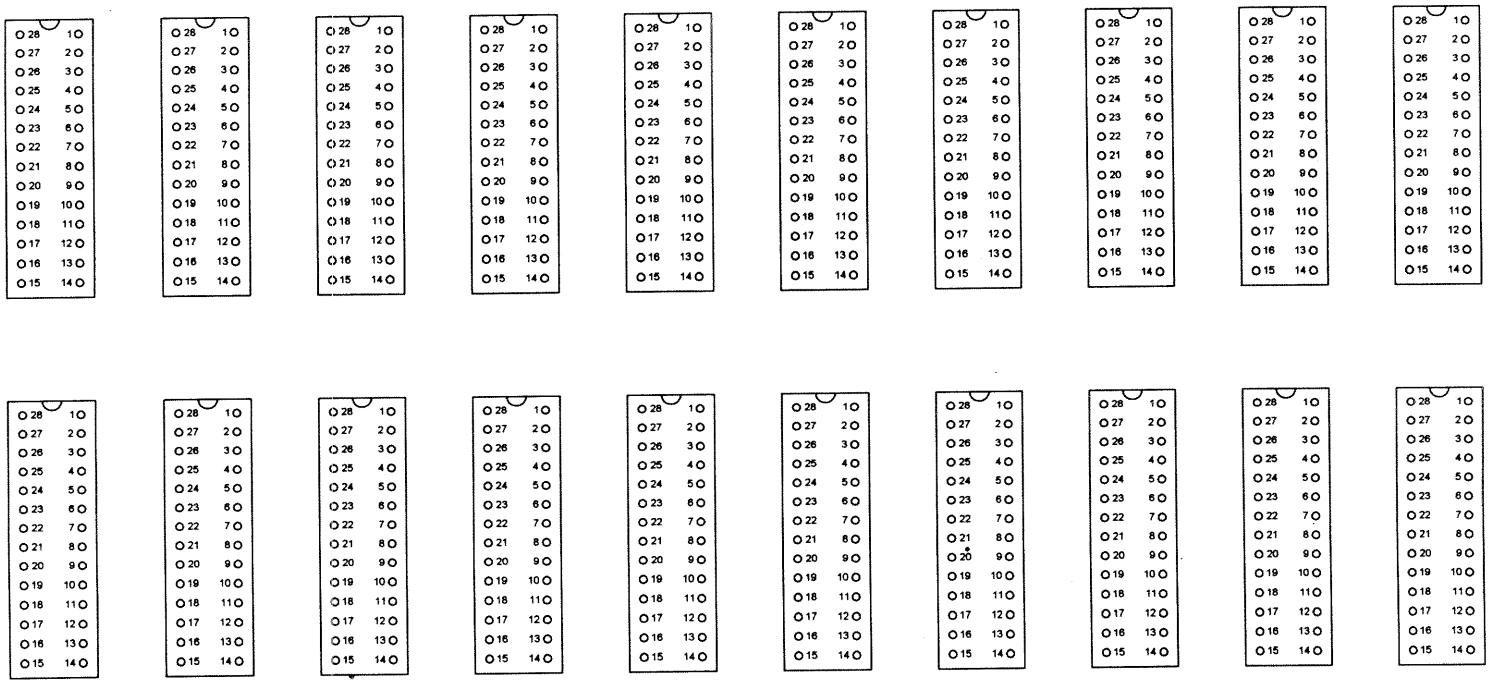
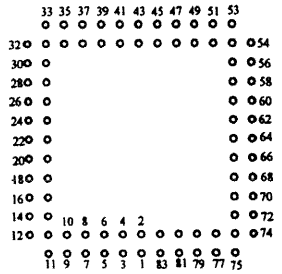


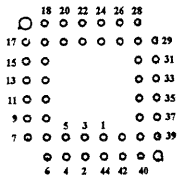

28 1
27 2
26 3
25 4
24 5
23 6
22 7
21 8
20 9
19 10
18 11
17 12
16 13
15 14

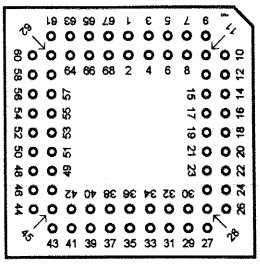
Set fra wrapside

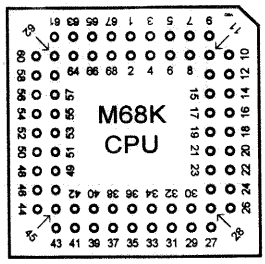
84 Pins

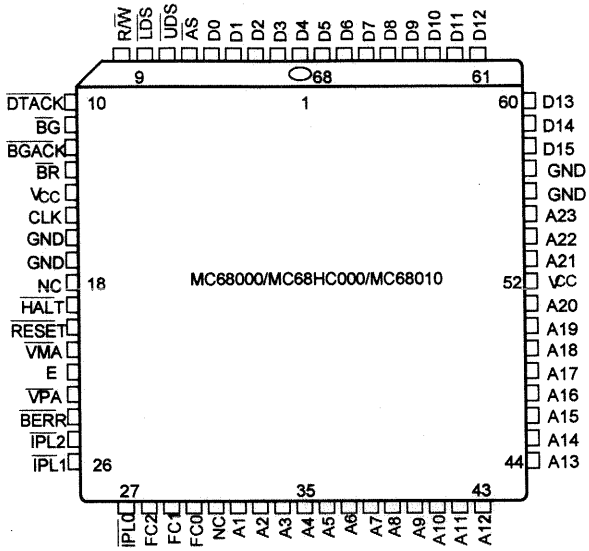


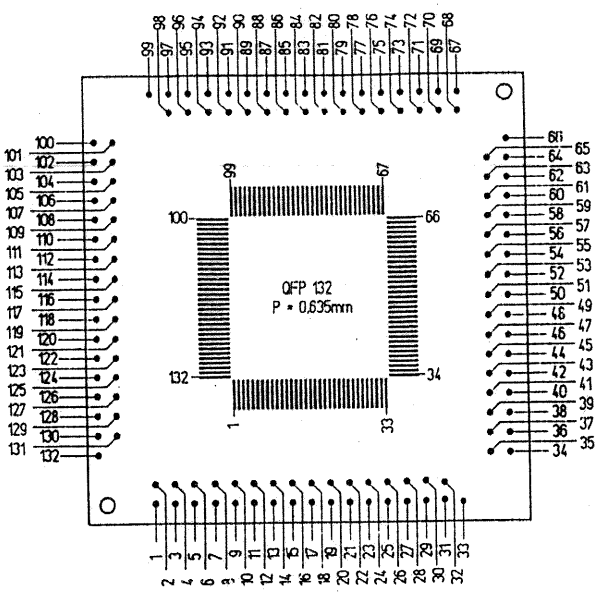
44 Pins

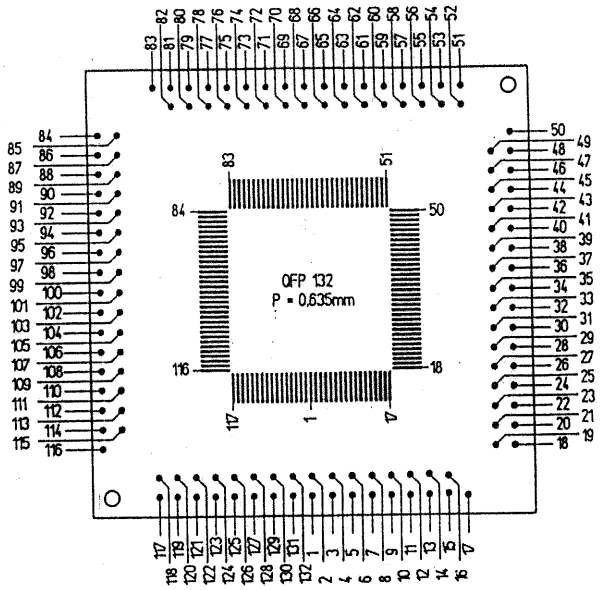




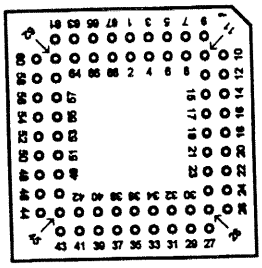

M68K
CPU


R/W
LDS
UDS
AS
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
9
68
61
DTACK
10
1
60
D13
BG
D14
BGACK
D15
BR
GND
VCC
GND
CLK
A23
GND
A22
GND
A21
NC
18
MC68000/MC68HC000/MC68010
52
VCC
HALT
A20
RESET
A19
VMA
A18
E
A17
VPA
A16
BERR
A15
IPL2
A14
IPL1
26
44
A13
27
35
43
IPL0
FC2
FC1
FC0
NC
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12

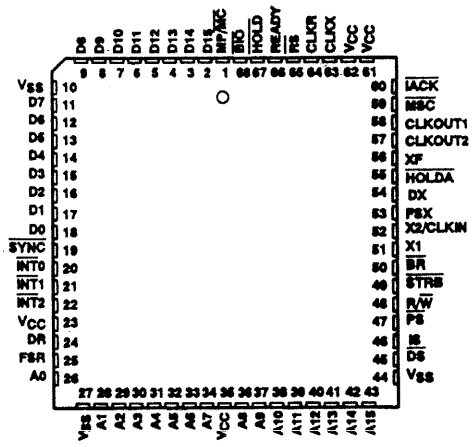

QFP 132
P = 0,635mm


QFP 132
P = 0,635mm

SMJ320C26
DIGITAL SIGNAL PROCESSOR



68-PIN FJ AND FD
LEADED AND LEADLESS
CERAMIC CHIP CARRIER PACKAGES†
(TOP VIEW)



† See Pin Assignments Table (Page 2) and Pin Nomenclature Table (Page 3) for location and description of all pins.

PIN NOMENCLATURE

NAME	I/O/Z†	DEFINITION
V_{CC}	I	5-V supply pins.
V_{SS}	I	Ground pins.
X1	O	Output from internal oscillator for crystal.
X2/CLKIN	I	Input to internal oscillator from crystal or external clock.
CLKOUT1	O	Master clock output (crystal or CLKIN frequency/4).
CLKOUT2	O	A second clock output signal.
D15–D0	I/O/Z	16-bit data bus D15 (MSB) through D0 (LSB). Multiplexed between program, data and I/O spaces.
A15–A0	O/Z	16-bit address bus A15 (MSB) through A0 (LSB).
$\overline{PS}$, $\overline{DS}$, $\overline{IS}$	O/Z	Program, data and I/O space select signals.
R/$\overline{W}$	O/Z	Read/write signal.
$\overline{STRB}$	O/Z	Strobe signal.
$\overline{RS}$	I	Reset input.
$\overline{INT2}$, $\overline{INT1}$, $\overline{INT0}$	I	External user interrupt inputs.
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select pin.
$\overline{MSC}$	O	Microstate complete signal.
$\overline{IACK}$	O	Interrupt acknowledge signal.
READY	I	Data ready input. Asserted by external logic when using slower devices to indicate that the current bus transaction is complete.
$\overline{BR}$	O	Bus request signal. Asserted when the SMJ320C26 requires access to an external global data memory space.
XF	O	External flag output (latched software – programmable signal).
$\overline{HOLD}$	I	Hold input. When asserted, SMJ320C26 goes into an idle mode and places the data address and control lines in the high-impedance state.
$\overline{HOLDA}$	O	Hold acknowledge signal.
$\overline{SYNC}$	I	Synchronization input.
$\overline{BIO}$	I	Branch control input. Polled by BIOZ instruction.
DR	I	Serial data receive input.
CLKR	I	Clock input for serial port receiver.
FSR	I	Frame synchronization pulse for receive input.
DX	O/Z	Serial data transmit output.
CLKX	I	Clock input for serial port transmitter.
FSX	I/O/Z	Frame synchronization pulse for transmit. May be configured as either an input or an output.

† I/O/Z denotes input/output/high-impedance state.