SERIES 55450B/75450B DUAL PERIPHERAL DRIVERS

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PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT HIGH SPEEDS

performance

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 20 V
- High-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 55450/75450

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55450B	AND†	J
SN55451B	AND	JG
SN55452B	NAND	JG
SN55453B	OR	JG
SN55454B	NOR	JG
SN75450B	AND†	J, N
SN75451B	AND	JG, P
SN75452B	NAND	JG, P
SN75453B	OR	JG, P
SN75454B	NOR	JG, P

†With output transistor base connected externally to output of gate.

description

Series 55450B/75450B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. The 55450B/75450B family is functionally interchangeable with and replaces the 75450 family and the 75450A family devices manufactured previously. The speed of the 55450B/75450B family is equal to that of the 75450 family and a test to ensure freedom from latch-up has been added. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers. lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55450B drivers are characterized for operation over the full military temperature range of −55°C to 125°C; Series 75450B drivers are characterized for operation from 0°C to 70°C.

The SN55450B and SN75450B are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55450B	SN55451B SN55452B SN55453B SN55454B	SN75450B	SN75451B SN75452B SN75453B SN75454B	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	7	7	V
Input voltage		5.5	5.5	5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	5.5	5.5	V
V_{CC}-to-substrate voltage		35		35		V
Collector-to-substrate voltage		35		35		V
Collector-base voltage		35		35		V
Collector-emitter voltage (see Note 3)		30		30		V
Emitter-base voltage		5		5		V
Off-state output voltage			30		30	V
Continuous collector or output current (see Note 4)		400	400	400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4)		500	500	500	500	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	J package	1375		1025		mW
	JG package		1050		825	
	N package			1150		
	P package				1000	
Operating free-air temperature range		−55 to 125	−55 to 125	0 to 70	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J or JG package	300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 21. In the J and JG packages, SN55450B through SN55454B chips are alloy-mounted; SN75450B through SN75454B chips are glass-mounted.

recommended operating conditions (see Note 6)

	SERIES 55450B			SERIES 75450B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 6: For the SN55450B and SN75450B only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

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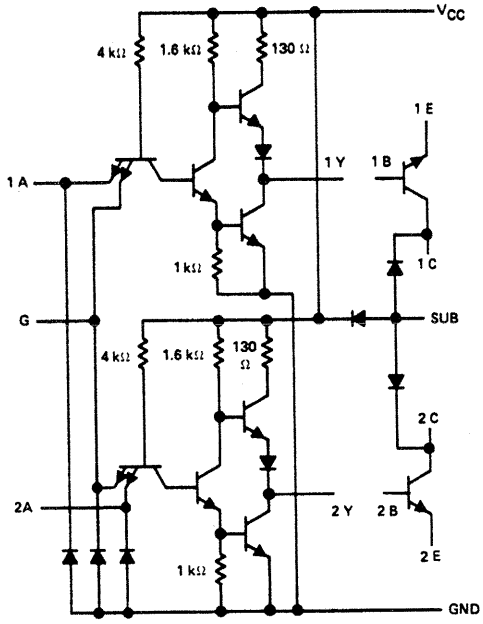
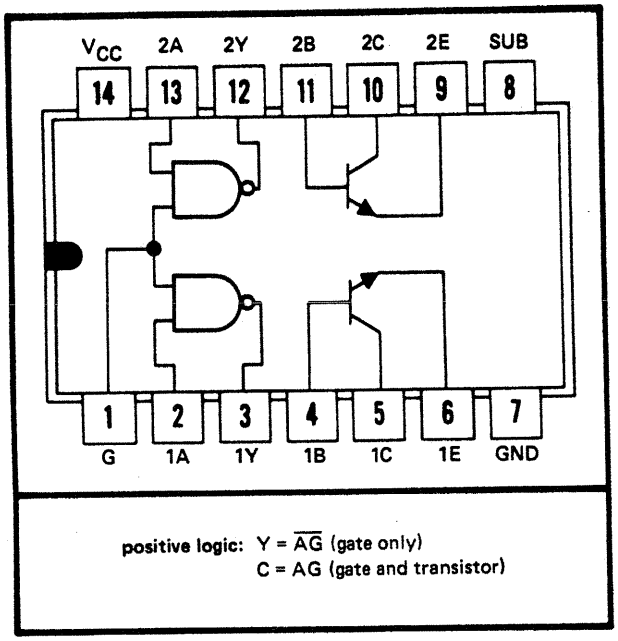
schematic



Resistor values shown are nominal.

SN55450B . . . J
SN75450B . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER			TEST CONDITIONS†	SN55450B MIN	SN55450B TYP‡	SN55450B MAX	SN75450B MIN	SN75450B TYP‡	SN75450B MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.25	0.5		0.25	0.4	V
I_I	Input current at maximum input voltage	input A	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
		input G				2			2	
I_{IH}	High-level input current	input A	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		input G				80			80	
I_{IL}	Low-level input current	input A	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		input G				−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18	−35	−55	−18	−35	−55	mA
I_{CCH}	Supply current, outputs high		V_{CC} = MAX, V_I = 0		2.8	4		2.8	4	mA
I_{CCL}	Supply current, outputs low		V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS†		SN55450B			SN75450B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0		35			35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		30			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C	See Note 7	25			25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			30			
		V_{CE} = 3 V, I_C = 100 mA, T_A = MIN		10			20			
		V_{CE} = 3 V, I_C = 300 mA, T_A = MIN		15			25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA, I_C = 100 mA	See Note 7		0.85	1.2		0.85	1	V
		I_B = 30 mA, I_C = 300 mA			1	1.4		1	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA, I_C = 100 mA	See Note 7		0.25	0.5		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA			0.45	0.8		0.45	0.7	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 7: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Figure 1		12	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	15	ns

output transistors

PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_d	Delay time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, C_L = 15 pF, R_L = 50 Ω, See Figure 2		8	15	ns
t_r	Rise time			12	20	ns
t_s	Storage time			7	15	ns
t_f	Fall time			6	15	ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor paramters.

gates and transistors combined

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_C ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	30	ns
t_{TLH}	Transition time, low-to-high-level output			7	12	ns
t_{THL}	Transition time, high-to-low-level output			9	15	ns
V_{OH}	High-level output voltage after switching	V_S = 20 V, I_C ≈ 300 mA, R_{BE} = 500 Ω, See Figure 4	V_S−6.5			mV

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