DESCRIPTION
The NE/SE564 is a versatile, high guaranteed frequency phase-locked loop designed for operation up to 50MHz. As shown in the Block Diagram, the NE/SE564 consists of a VCO, limiter, phase comparator, and post detection processor.

FEATURES
- Operation with single 5V supply
- TTL-compatible inputs and outputs
- Guaranteed operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (externally controlled)

APPLICATIONS
- High speed modems
- FSK receivers and transmitters
- Frequency Synthesizers

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
<th>ORDER CODE</th>
<th>DWG #</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-Pin Plastic Small Outline (SO) Package</td>
<td>0 to +70°C</td>
<td>NE564D</td>
<td>SOT109-1</td>
</tr>
<tr>
<td>16-Pin Plastic Dual In-Line Package (DIP)</td>
<td>0 to +70°C</td>
<td>NE564N</td>
<td>SOT38-4</td>
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<tr>
<td>16-Pin Plastic Dual In-Line Package (DIP)</td>
<td>-55 to +125°C</td>
<td>SE564N</td>
<td>SOT38-4</td>
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</table>

BLOCK DIAGRAM

Figure 1. Pin Configuration

Figure 2. Block Diagram
### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>RATING</th>
<th>UNITS</th>
</tr>
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<tbody>
<tr>
<td>V+</td>
<td>Supply voltage</td>
<td>14</td>
<td>V</td>
</tr>
<tr>
<td>IOUT</td>
<td>Sink Max (Pin 9) and sourcing (Pin 11)</td>
<td>11</td>
<td>mA</td>
</tr>
<tr>
<td>IBIAS</td>
<td>Bias current adjust pin (sinking)</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>P_D</td>
<td>Power dissipation</td>
<td>600</td>
<td>mW</td>
</tr>
<tr>
<td>T_A</td>
<td>Operating ambient temperature</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>T_STG</td>
<td>Storage temperature range</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

**NOTE:**
Operation above 5V will require heatsinking of the case.

### DC AND AC ELECTRICAL CHARACTERISTICS

**VCC = 5V; TA = 0 to 25°C; fO = 5MHz, I2 = 400μA; unless otherwise specified.**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>LIMITS</th>
<th>LIMITS</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>SE564</td>
<td>NE564</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Maximum VCO frequency</td>
<td>C1 = 0 (stray)</td>
<td>50</td>
<td>65</td>
</tr>
<tr>
<td></td>
<td>Lock range</td>
<td>Input ≥ 200mVRMS</td>
<td>40</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TA = 25°C</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TA = 125°C</td>
<td>50</td>
<td>80</td>
</tr>
<tr>
<td></td>
<td>Capture range</td>
<td>fO = 5MHz</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>fO = 5MHz</td>
<td>500</td>
<td>1500</td>
</tr>
<tr>
<td></td>
<td></td>
<td>fO = 5MHz</td>
<td>300</td>
<td>800</td>
</tr>
<tr>
<td></td>
<td>VCO free-running frequency</td>
<td>C1 = 91pF, RC = 100Ω &quot;Internal&quot;</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>VCO frequency change with supply voltage</td>
<td>VCC = 4.5V to 5.5V</td>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Demodulated output voltage</td>
<td>Modulation frequency: 1kHz</td>
<td>16</td>
<td>28</td>
</tr>
<tr>
<td></td>
<td></td>
<td>fO = 5MHz, input deviation:</td>
<td>8</td>
<td>14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2%T = 25°C</td>
<td>8</td>
<td>14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1%T = 125°C</td>
<td>12</td>
<td>16</td>
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<tr>
<td></td>
<td></td>
<td>1%T = 0°C</td>
<td>6</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1%T = -55°C</td>
<td>6</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Distortion</td>
<td>Deviation: 1% to 8%</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>S/N</td>
<td>Signal-to-noise ratio</td>
<td>Std. condition, 1% to 10% dev.</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td>AM rejection</td>
<td>Std. condition, 30% AM</td>
<td>35</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td>Demodulated output at operating voltage</td>
<td>Modulation frequency: 1kHz</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>fO = 5MHz, input deviation:</td>
<td>8</td>
<td>14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCC = 4.5V</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCC = 5.5V</td>
<td>8</td>
<td>14</td>
</tr>
<tr>
<td></td>
<td>I_CC</td>
<td>Supply current</td>
<td>VCC = 5V I1, I10</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td>Output</td>
<td>VOUT = 5V, Pins 16, 9</td>
<td>1</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IOUT = 2mA, Pins 16, 9</td>
<td>0.3</td>
<td>0.6</td>
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<tr>
<td></td>
<td></td>
<td>IOUT = 6mA, Pins 16, 9</td>
<td>0.4</td>
<td>0.8</td>
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</table>
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3. Typical Performance Characteristics
Typical Performance Characteristics (Continued)

Variation of the Comparator’s Output Voltage vs Phase Error and Bias Current ($K_D$)

VCO Output Frequency as a Function of Input Voltage and Bias Current ($K_O$)

Figure 4. Typical Performance Characteristics (cont.)

Test Circuit

Figure 5. Test Circuit
FUNCTIONAL DESCRIPTION

(Figure 6)
The NE564 is a monolithic phase-locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz.

In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output of the PLL can be written as shown in the following equation:

$$V_O = \frac{f_{IN} - f_O}{K_{VCO}}$$  \hspace{1cm} (1)

$$K_{VCO} = \text{conversion gain of the VCO}$$

$$f_{IN} = \text{frequency of the input signal}$$

$$f_O = \text{free-running frequency of the VCO}$$

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of $f_{IN}$ from $f_O$. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at Pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free-running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the DC levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrowband signals where the deviation in $f_{IN}$ itself may be less than the change in $f_O$ due to temperature. This effect can be eliminated if the DC or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the DC levels of the PLL output do not affect the FSK output.

VCO Section
Due to its inherent high-frequency performance, an emitter-coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q21 and Q23 with current sources Q25 - Q26 form the basic oscillator. The approximate free-running frequency of the oscillator is shown in the following equation:

$$f_O \approx \frac{1}{22R_C(C_1 + C_S)}$$  \hspace{1cm} (2)

$$R_C = R_{19} = R_{20} = 100\Omega \text{ (INTERNAL)}$$

$$C_1 = \text{external frequency setting capacitor}$$

$$C_S = \text{stray capacitance}$$

Variation of $V_C$ (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the monolithic resistor. To compensate for this, a current $I_C$ with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section
The phase detection processor consists of a doubled-balanced modulator with a limiter amplifier to improve AM rejection. Schottky-clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q4 and Q15 which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at Pin 2.

Post Detection Processor Section
The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a DC retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the DC retriever is formed by the transconductance amplifier Q22 - Q23 together with an external capacitor which is connected at the amplifier output (Pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$\frac{dV_O}{dt} = g_M \frac{V_{IN}}{C_2}$$  \hspace{1cm} (3)

$$g_M = \text{transconductance of the amplifier}$$

$$C_2 = \text{capacitor at the output (Pin 14)}$$

$$V_{IN} = \text{signal voltage at amplifier input}$$

With proper selection of $C_2$, the integrator time constant can be varied so that the output voltage is the DC or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of Q49 - Q50 with positive feedback being provided by Q47 - Q48. The hysteresis is varied by changing the current in Q32 with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a DC control, provides symmetric variation around the nominal value.

Design Formula
The free-running frequency of the VCO is shown by the following equation:

$$I_O = \frac{1}{22R_C(C_1 + C_S)}$$  \hspace{1cm} (4)

$$R_C = 100\Omega$$

$$C_1 = \text{external cap in farads}$$

$$C_S = \text{stray capacitance}$$

The loop filter diagram shown is explained by the following equation:

$$f_S = \frac{1}{T + sR_C3} \text{ (First Order)}$$  \hspace{1cm} (5)

$$R = R_{12} = R_{13} = 1.3k\Omega \text{ (Internal)}$$

*Refer to Figure 6.

NOTE:
EQUIVALENT SCHEMATIC

Figure 6. Equivalent Schematic

Figure 7. FM Demodulator at 5V
APPLICATIONS

FM Demodulator
The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in Figures 7 and 8, respectively. The input signal is AC coupled with the output signal being extracted at Pin 14. Loop filtering is provided by the capacitors at Pins 4 and 5 with additional filtering being provided by the capacitor at Pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be 1% or higher.

Modulation Techniques
The NE564 phase-locked loop can be modulated at either the loop filter ports (Pins 4 and 5) or the input port (Pin 6) as shown in Figure 9. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in Figure 10. This curve will be appropriate for signals injected into Pins 4 and 5 as shown in Figure 9.

FSK Demodulation
The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high-frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 10 shows a high-frequency FSK decoder designed for input frequency deviations of ±1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from Figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune fO' 10.8MHz.

OUTLINE OF SETUP PROCEDURE

1. Determine operating frequency of the VCO: IF÷N in feedback loop, then
   \( f_O = N \times f_{IN} \).

2. Calculate value of the VCO frequency set capacitor:
   \( C_O = \frac{1}{2200 f_O} \).

3. Set I2 (current sinking into Pin 2) for \( \approx 100\mu A \). After operation is obtained, this value may be adjusted for best dynamic behavior, and replace with fixed resistor value of \( R_2 = \frac{V_{CC} - 1.3V}{I_B} \).

4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to φ det.). Adjust \( C_O \) trim or frequency adj. Pins 4 - 5 for exact center frequency, if needed.

5. Close loop and inject input signal to Pin 6. Monitor Pins 3 and 6 with two-channel scope. Lock should occur with \( \Delta\phi - \phi \) equal to 90° (phase error).
6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pins 4 and 5. (See PLL application section)
7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not 50% in duty cycle, DC offsets will occur in the loop which tend to create an artificial or biased VCO.
8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10 - 50µF on Pins 4, 5. Also, careful supply decoupling may be necessary. This includes the counter chain VCC lines.

*NOTE: Use R9-11 only if rise time is critical.

Figure 10. 10.8MHz FSK Decoder Using the 564
Figure 11. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs

NOTES:
1. Top trace = Pin 4
2. Center trace = Pin 5
3. Bottom trace = Pin 16

Figure 12. NE564 Phase-Locked Frequency Multiplier

*NOTE:
Use R9-11 only if rise time is critical.