FSK Modulator/Demodulator

GENERAL DESCRIPTION

The XR-210 is a highly versatile monolithic phase-locked loop system, especially designed for data communications. It is particularly well suited for FSK modulation/demodulation (MODEM) applications, frequency synthesis, tracking filters, and tone decoding. The XR-210 operates over a power supply range of 5V to 26V, and over a frequency band of 0.5 Hz to 20 MHz. The circuit can accommodate analog signals between 300μV and 3V, and can interface with conventional DTL, TTL, and ECL logic families.

FEATURES

Wide Frequency Range	0.5Hz to 20MHz
Wide Supply Voltage Range	5V to 26V
Digital Programming Capability	
RS-232C Compatible Demodulator Output	
DTL, TTL and ECL Logic Compatibility on Inputs	
Wide Dynamic Range	300μV to 3V
ON-OFF Keying & Sweep Capability	
Wide Tracking Range	±1% to ±50%
Good Temperature Stability	200 ppm/°C
High-Current Logic Output	50mA
Independent "Mark" and "Space" Frequency Adjustment	
VCO Duty Cycle Control	

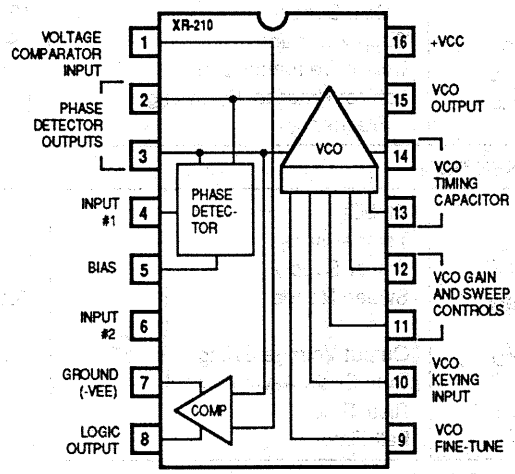
APPLICATIONS

Data Synchronization
Signal Conditioning
FSK Generation
Tone Decoding
Frequency Synthesis
FSK Demodulation
Tracking Filter
FM Detection
FM and Sweep Generation
Wideband Discrimination

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation	750mW
Derate Above + 25°C	6.0mW/°C
Storage Temperature	65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-210M	Ceramic	–55°C to +125°C
XR-210CN	Ceramic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-210 is made up of a stable wide-range voltage- controlled oscillator (VCO), exclusive OR gate type phase detector, and an analog voltage comparator. The VCO, which produces a square wave as an output, is either used in conjunction with the phase detector to form a phase-locked loop (PLL) for FSK demodulation and tone detection or as a generator in FSK modulation schemes. The phase detector when used in the PLL configuration produces a differential output voltage with a 6 KΩ output impedance, which when capacitively loaded forms a single pole loop filter. The voltage comparator is used to sense the phase detector output and produces the output in the FSK demodulation connection.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = 12V$ (single supply), $T_A = +25°C$, Test circuit of Figure 1 with $C_O = 0.02\mu F$, S_1, S_2, S_5 closed, S_3, S_4, S_6, S_7 open, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS						
V_{CC}	Supply Voltage					
	Single Supply	5		26	V dc	See Figure 1
	Split Supply	±2.5		113	V dc	See Figure 2
I_{CC}	Supply Current	9	12	16	mA	See Figure 1, S_2 open
f_{UL}	Upper Frequency Limit	15	20		MHz	See Figure 1, S_1 open, S_4 closed
f_{LL}	Lowest Practical Operating Frequency		0.5		Hz	$C_O = 500\mu F$ non polarized
VCO SECTION						
	Stability					
T_C	Temperature		200	500	ppm/°C	f = 10 kHz, $V^+ \geq 10V$, $0 < T_T < 70°C$*
PSR	Power Supply		0.05	0.5	%/V	$10V < V^+ < 24V$
f_{SW}	Sweep Range	5:1	8:1			S_3 closed, S_4 Open, $0 < V_S < 6V$ See Figure 5, $V^+ = 12V$
V_O	Output Voltage Swing	1.5	2.5		V p-p	S_5 open
DC	Duty Cycle Asymmetry		±1	±3	%	S_5 open
T_R	Rise Time		20		ns	10 pF to ground at Pin 15, S_5 open
T_F	Fall Time		40		ns	10 pF to ground at Pin 15, S_5 open
PHASE DETECTOR SECTION						
K_D	Conversion Gain		2		V/rad	$V_{IN} > 50mV$ rms, see Figure 8
Z_O	Output Impedance		6		kΩ	Measured looking into Pin 2 or 3
V_{OOS}	Output Offset Voltage		35	150	mV	Measured across Pin 1 and 3, $V_{IN} = 0$, S_5 open
VOLTAGE COMPARATOR SECTION						
A_{VOL}	Open Loop Voltage Gain	66	80		dB	f = 20Hz
Z_{IN}	Input Impedance	0.5	2		MΩ	Measured looking into Pin 1
V_{OS}	Input Offset Voltage		1		mV	
I_B	Input Bias Current		80		nA	
CMRR	Common Mode Rejection		90		dB	
LOGIC OUTPUT SECTION						
SR	Slew Rate		15		V/μsec	$R_L = 3k\Omega$, $C_L = 10pF$, S_2 closed
I_{OL}	"1" Output Leakage Current		0.02	10	μA	$V_O = +24V$
V_{OL}	"0" Output Voltage		0.2	0.4	V	$I_L = 10mA$
I_{SINK}	Current Sink Capability	30	50		mA	$V_O \leq 1V$

*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

PRINCIPLES OF OPERATION

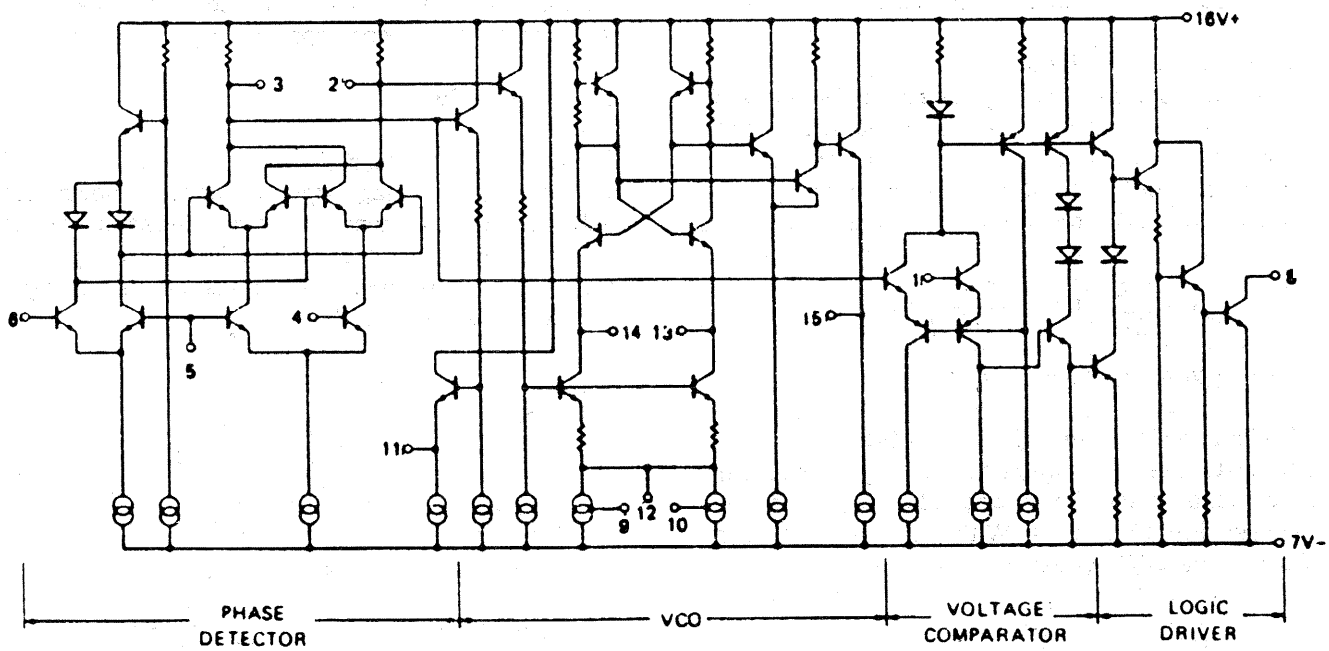
Description of Controls

Phase-Detector Inputs (Pin 4 and 6):
One input to the phase detector is used as the signal input; the remaining input should be ac coupled to the VCO output (Pin 15), to complete the PLL (see Figure 1). For split supply operation, these inputs are biased from ground as shown in Figure 2.

Phase-Detector Bias (Pin 5):
This terminal should be dc biased as shown in Figures 1 and 2, and ac grounded with a bypass capacitor. The bias resistor in series with this pin should be half the value as those in series with Pin 4 and 6.

Phase-Detector Outputs (Pin 2 and 3):
The low-frequency (or dc) voltage across these pins corresponds to the phase difference between the two signals at the phase-detector inputs (Pin 4 and 6).

EQUIVALENT SCHEMATIC DIAGRAM



These differential phase-detector outputs are internally connected to the VCO control terminals. Pin 3 is also internally connected to the reference input of the voltage comparator section.

In normal use, the low-pass loop-filter capacitor, C_1, is connected between Pin 2 and 3. The 6 kΩ impedances of the two outputs add to 12 kΩ in the single-pole RC low-pass loop filter. Pin 2 is externally connected to the voltage comparator input (Pin 1) through an RC low-pass filter.

Frequency-Keying Input (Pin 10):
The VCO frequency can be varied between two discrete frequencies, f_1 and f_2, by connecting an external resistor, R_X, to this terminal, Referring to Figure 6, the VCO frequency is proportional to the sum of currents, I_1 and I_2, through the transistors, T_1 and T_2, on the monolithic chip. These transistors are biased from a fixed internal reference. The current, I_1, is set internally, and is partially controllable by the fine-tune adjustment, R_T. The current, I_2, is set by the external resistor, R_X, connected between Pin 10 and Pin 7. For any C_O setting, the VCO frequency, f_2, with R_X connected to Pin 10, can be expressed as:

$$f_2 = f_1 \left(1 + \frac{0.3}{R_X} \right) \text{Hz}$$

where f_1 is the frequency with Pin 10 open-circuited, and R_X is in kΩ. Note that f_2 can be fine-tuned to a desired value by the proper choice of R_X.

VCO Sweep input (Pin 12):
The VCO frequency can be swept over a broad range by applying an analog sweep voltage, V_S to Pin 12 (see Figure 5). The impedance level looking into the sweep input is approximately 50Ω. Therefore, for sweep applications, a current limiting resistor, R_S, should be connected in series with this terminal. Typical sweep characteristics of the circuit are shown in Figure 5. The VCO temperature dependence is minimal when the sweep input is not used, and should be left open-circuited.

CAUTION: For safe operation of the circuit, the maximum current, I_S, drawn from the sweep terminal should be limited to 5mA or less, under all operating conditions.

VCO Conversion Gain (Pin 11):
The VCO voltage-to-frequency conversion gain, K_O, is inversely proportional to the value of the external gain-control resistor, R_O, connected across Pin 11 and 12.

Fine Tune Control (Pin 9):
For a given choice of timing capacitor, C_O, the VCO frequency can be further fine-adjusted to a desired frequency, f_1, by means of a trimmer resistor, R_T, connected from Pin 9 to Pin 7, as shown in Figure 6. The fine tuned VCO frequency, f_1, is related to R_T as:

$$f_1 \approx \frac{220}{C_O}\left(1 + \frac{0.1}{R_T}\right) \text{Hz}$$

where C_O is in µF, and R_T is in kΩ.

VCO Timing Capacitor (Pin 13 and 14):
The VCO free-running frequency, f_0, is inversely proportional to the timing capacitor, C_O, connected between Pin 13 and 14. With Pin 9 and 10 open-circuited, the VCO frequency is related to C_O as:

$$f_0 \approx \frac{220}{C_O} \text{ Hz}$$

where C_O is in µF.

VCO Output (Pin 15):
The VCO produces approximately a 2.5V p-p square wave output signal at this pin. The dc output level is approximately 2 volts below V_{CC}. This pin should be connected to Pin 7 through a 10kΩ resistor to increase the output current drive capability. For high-voltage operation (V_{CC} > 20V), a 20kΩ resistor is recommended. It is also advisable to connect a 500Ω resistor in series with this output, for short-circuit protection. This output can drive a 10kΩ or larger load.

Using the frequency-keying control, the VCO frequency can also be stepped in a binary manner by applying a logic signal to Pin 10, as shown in Figure 6. For high-level logic inputs, the transistor, T_2, is turned off, R_X is effectively switched out of the circuit, and the VCO frequency is shifted from f_2 to f_1.

Voltage Comparator Input (Pin 1):
This pin provides the signal input to the voltage comparator section. The comparator section is normally used for post-demodulation slicing and pulse shaping. Normally, Pin 1 is connected to Pin 2 through a 15K external resistor, as shown in Figures 1 and 2. The input impedance level at this pin is approximately 2 MΩ.

Logic Driver Output (Pin 8):
This pin provides a binary logic output corresponding to the polarity of the input signal, at the voltage comparator inputs. It is an open-collector type stage with high-current sinking capability.

Definition of Terms

Phase-Detector Gain, K_d:
K_d is the output voltage from the phase detector per radian of phase difference at the phase-detector inputs (Pin 4 and 6). K_d is proportional to the input signal for low-level inputs (≤25mV rms), and is constant at high-input levels (see Figure 8).

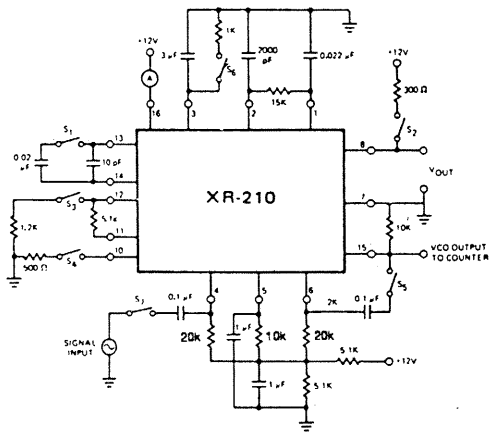


Figure 1. Test Circuits for Single Supply Operation

VCO Conversion Gain, K_O:

$$K_O \approx \frac{700}{C_O R_O} \text{ (radians/sec)/volt}$$

where C_O is in µF and R_O is in kΩ. For most applications, recommended values for R_O range from 1 kΩ to 10 kΩ.

When the XR-210 is connected as a PLL, its lock range can be controlled by varying the VCO gain control resistor, R_O, across Pin 11 and 12. For input signals greater than 30 mV rms, the PLL loop-gain is independent of signal amplitude, but is inversely proportional to R_O. Figure 7 shows the dependence of lock range, $\pm\Delta f_L$, on R_O.

Lock Range ($\Delta\omega_L$):
The range of frequencies in the vicinity of f_0 over which the PLL can maintain lock with an input signal. If saturation or limiting does not occur, the lock range is equal to the loop gain; i.e., $\Delta\omega L = K_T = K_d K_O$.

Capture Range ($\Delta\omega_C$):
The band of frequencies in the vicinity of fo where the PLL can establish or acquire lock with an input signal. It is also known as the acquisition range. It is always smaller than the lock range, and is related to the low-pass filter bandwidth. It can be approximated by a parametric equation of the form:

$$\Delta\omega_C \approx \Delta\omega_L |F(j\Delta\omega_C)|$$

where $|F(j\Delta\omega_C)|$ is the low-pass filter magnitude response at $\omega = \Delta\omega_C$. For a simple lag filter, it can be expressed as:

$$\Delta\omega_C \approx \sqrt{\frac{\Delta\omega_L}{T_1}}$$

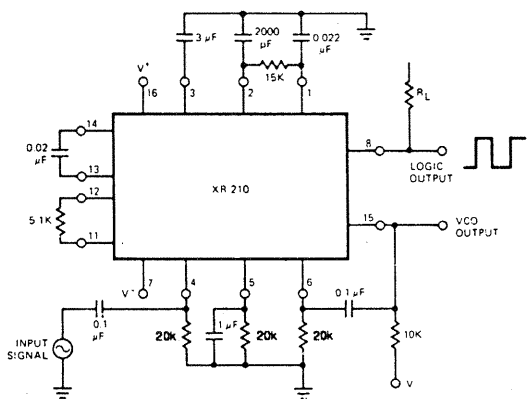


Figure 2. Test Circuit for Split Supplt Operation

APPLICATIONS INFORMATION

FSK Demodulation

Figure 3 shows a generalized circuit connection for FSK demodulation. The circuit is connected as a PLL system, by ac coupling the VCO output (Pin 15) to Pin 6. The FSK input is applied to Pin 4. When the input frequency is shifted, corresponding to a data bit, the polarity of the dc voltage across the phase-detector outputs (Pin 2 and 3) is reversed. The voltage comparator and the logic driver section convert this dc level shift to a binary pulse. The capacitor, C_1, serves as the PLL loop filter, and C_2 and C_3 as post-detection filters. The timing capacitor, C_O, and fine-tune adjustments are used to set the VCO frequency, f_0, midway between the mark and space frequencies of the input signal. Typical component values for 300 baud (103-type) and 1200 baud (202-type) MODEM applications are listed below:

OPERATING CONDITIONS		TYPICAL COMPONENT VALUES
300 Baud		
Low Band:	f_1 = 1070Hz	R_0 = 5.1kΩ, C_0 = 0.22µF
	f_2 = 1270Hz	$C_1 = C_2$ = 0.047µF, C_3 = 0.033µF
High Band:	f_1 = 2025Hz	R_0 = 8.2kΩ, C_0 = 0.1µF
	f_2 = 2225Hz	$C_1 = C_2 = C_3$ = 0.033µF
1200 Baud		
	f_1 = 1200Hz	C_1 = 0.033µF, C_3 = 0.02µF
	f_2 = 2200Hz	C_2 = 0.01µF

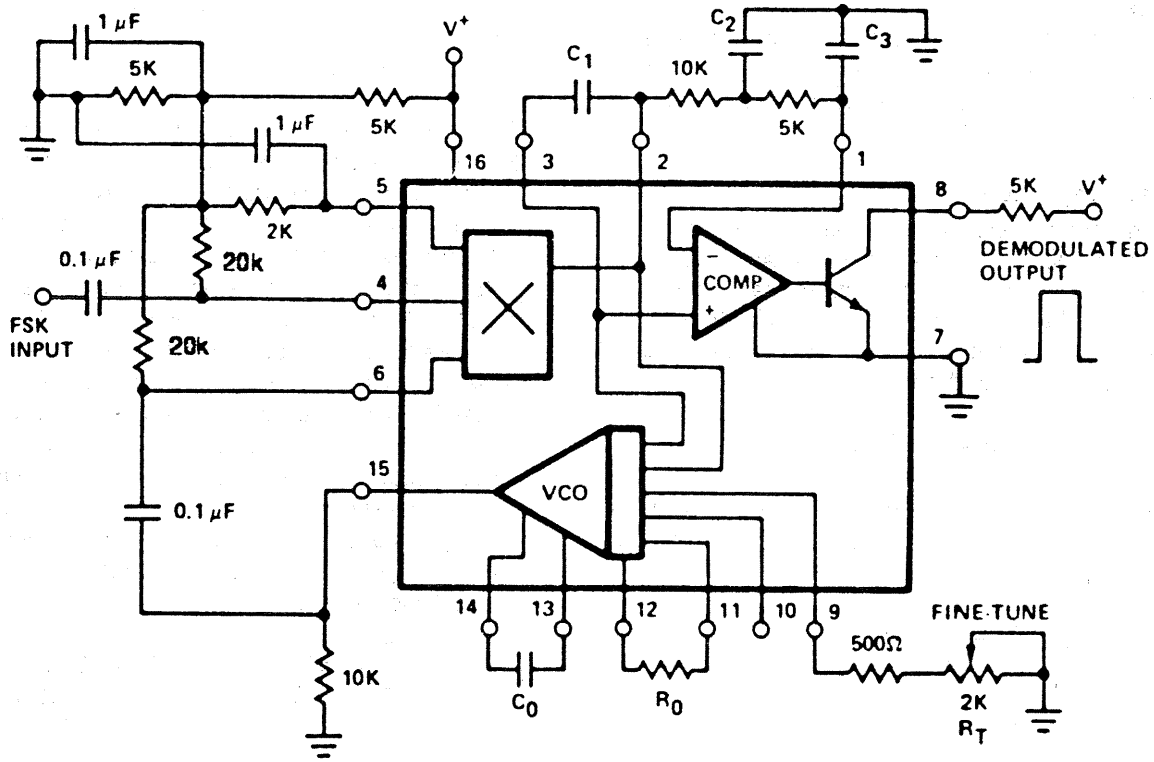


Figure 3. Circuit Connection for FSK Demodulation (Single Supply)

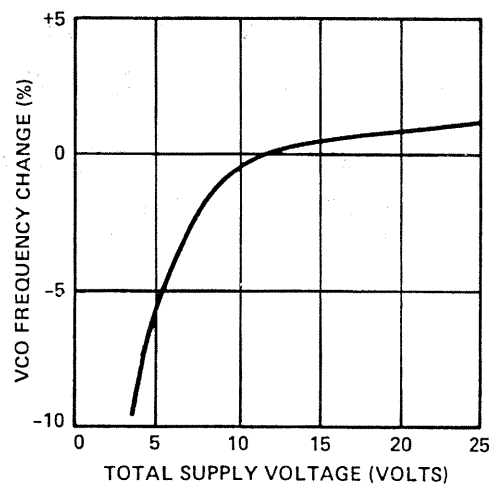
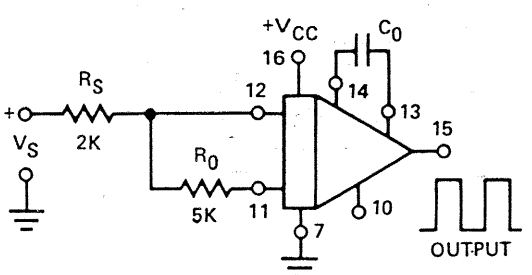


Figure 4. VCO Frequency Variation as a Function of Supply Voltage



(NOTE: $V_{SO} \approx V_{CC} - 5V$ = Open Circuit Voltage at pin 12)

Figure 5. Frequency Sweep Characteristics as a Function of Net Applied Sweep Voltage (Pin 10 Open)

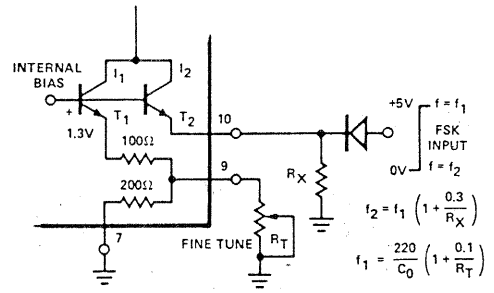


Figure 6. VCO Fine-Tune (Pin 9) and Frequency-Keying (Pin 10) Controls

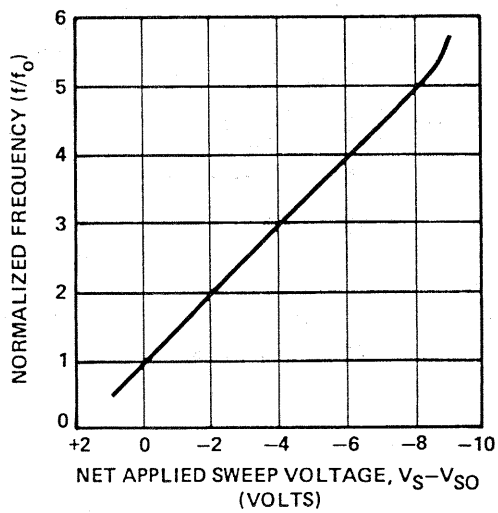


Figure 7.

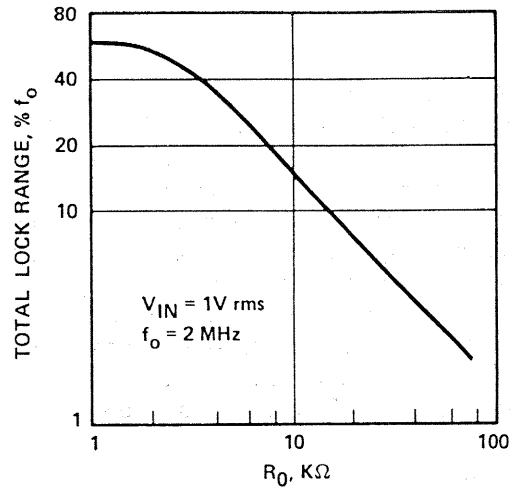


Figure 8. Total Lock Range, $\pm\Delta f_L$, versus VCO Gain Control Resistor, R_0

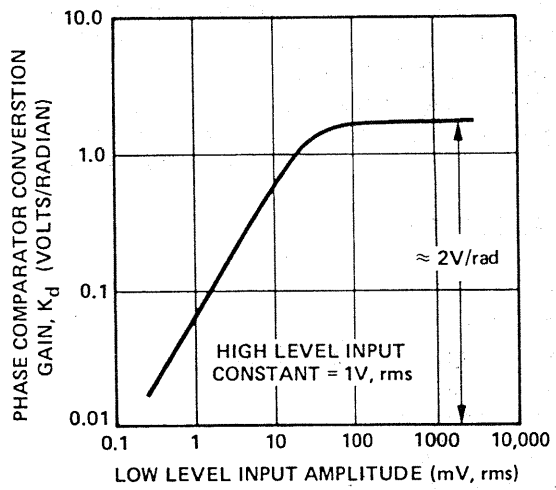


Figure 9. Phase Detector Conversion Gain, K_d, versus Input Amplitude