

# SN54HC160 THRU SN54HC163 SN74HC160 THRU SN74HC163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SCLS114 D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- Internal Look Ahead for Fast Counting
- Carry Output for N-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'HC160 and 'HC162 are decade counters, and the 'HC161 and 'HC163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

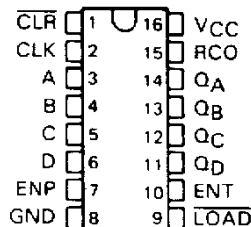
These counters are fully programmable; that is, they may be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the 'HC160 and 'HC161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

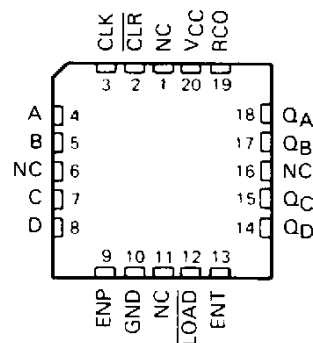
The clear function for the 'HC162 and 'HC163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next low-to-high transition of the clock input, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bits synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q<sub>A</sub> high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

SN54HC' . . . J PACKAGE  
SN74HC' . . . D OR N PACKAGE  
(TOP VIEW)



SN54HC' . . . FK PACKAGE  
(TOP VIEW)



NC—No internal connection

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**SN54HC160 THRU SN54HC163  
SN74HC160 THRU SN74HC163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

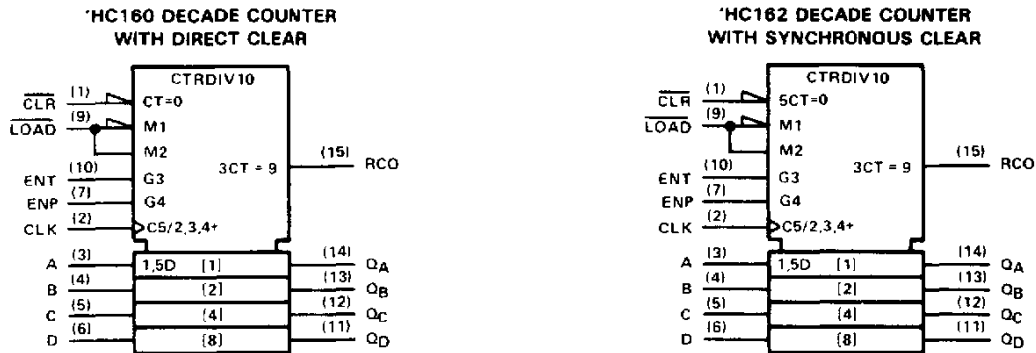
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These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{\text{LOAD}}$ ) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

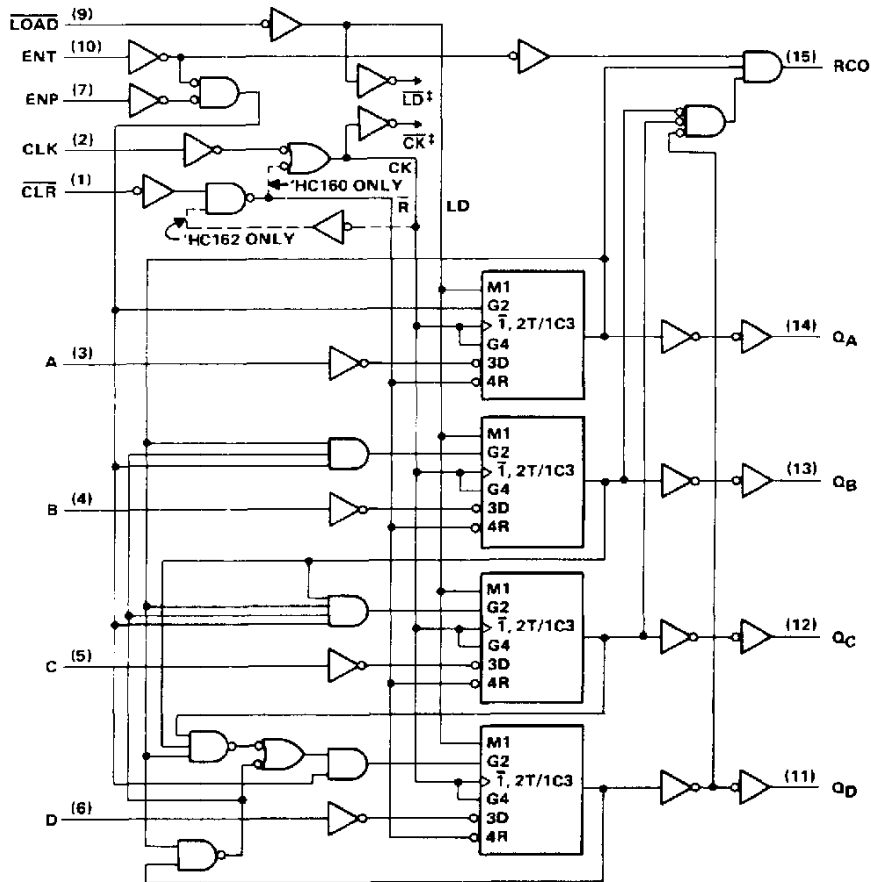
The SN54HC160 through SN54HC163 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC160 through SN74HC163 are characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**SN54HC160, SN54HC162  
SN74HC160, SN74HC162  
SYNCHRONOUS 4-BIT DECADE COUNTERS**

logic symbols<sup>†</sup>



'HC160 and 'HC162 logic diagram (positive logic)



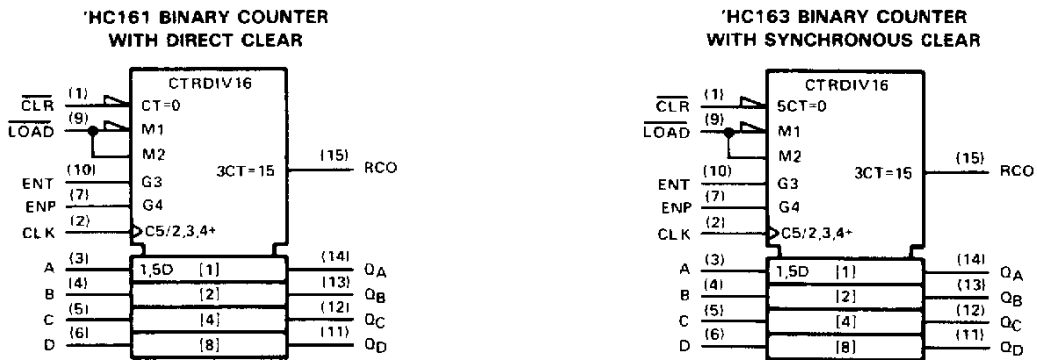
<sup>†</sup> These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

<sup>‡</sup> For the sake of simplicity, the routing of the complementary signals  $\overline{LD}$  and  $\overline{CK}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

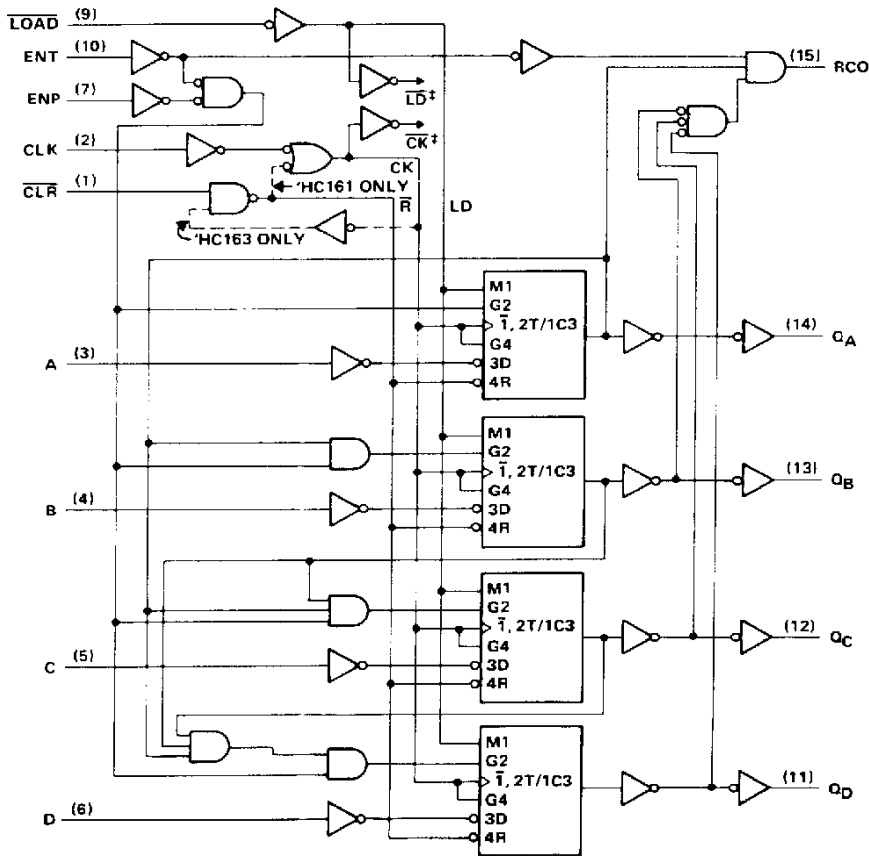
Pin numbers shown are for D, J, and N packages.

**SN54HC161, SN54HC163  
SN74HC161, SN74HC163  
SYNCHRONOUS 4-BIT BINARY COUNTERS**

logic symbols†



†'HC161 and †'HC163 logic diagram (positive logic)



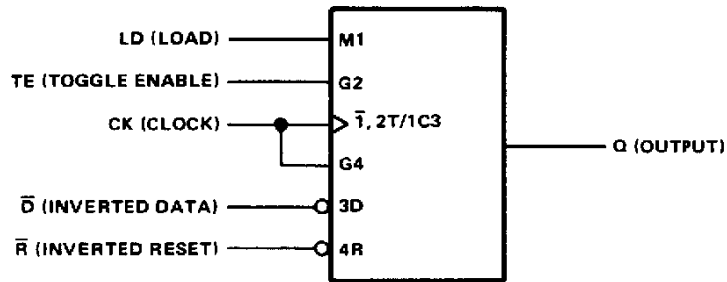
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

‡ For the sake of simplicity, the routing of the complementary signals  $\overline{LD}$  and  $\overline{CK}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

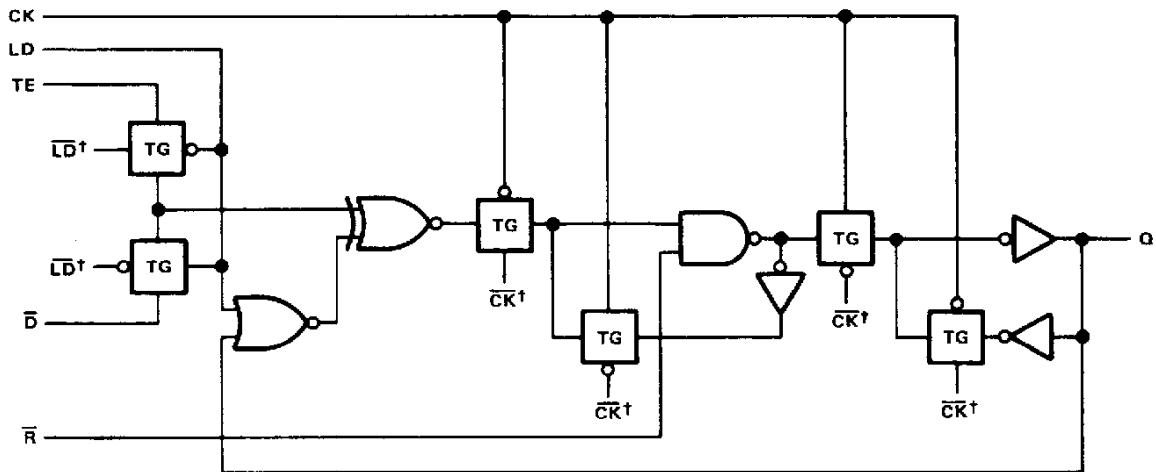
Pin numbers shown are for D, J, and N packages.

**SN54HC160 THRU SN54HC163  
SN74HC160 THRU SN74HC163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

logic symbol, each D/T flip-flop (positive logic)



logic diagram, each D/T flip-flop (positive logic)



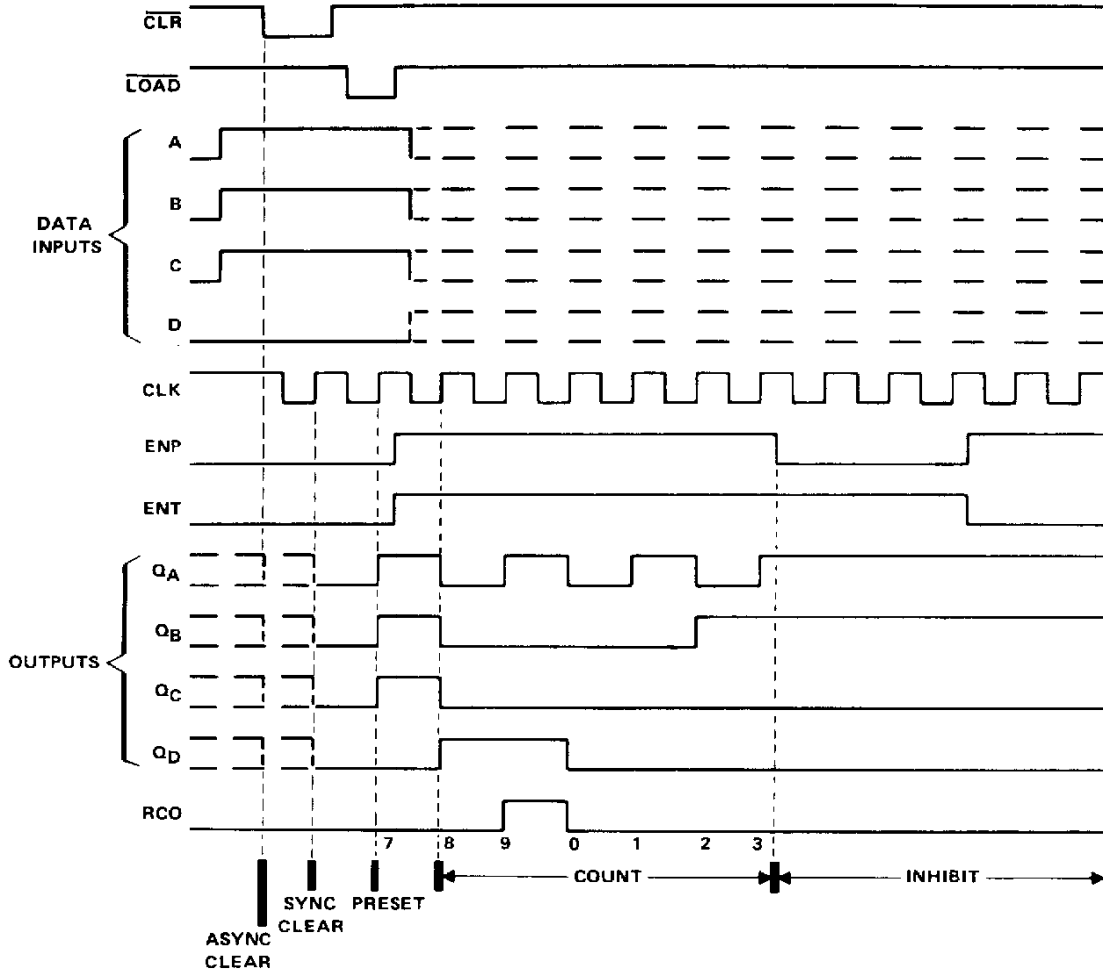
† The origins of the signals  $\overline{LD}$  and  $\overline{CK}$  are shown in the logic diagrams of the overall devices.

**SN54HC160, SN54HC162  
SN74HC160, SN74HC162  
SYNCHRONOUS 4-BIT DECADE COUNTERS**

**'HC160 and 'HC162 output sequence**

Illustrated below is the following sequence:

1. Clear outputs to zero (SN54HC160 and SN74HC160 are asynchronous; SN54HC162 and SN74HC162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

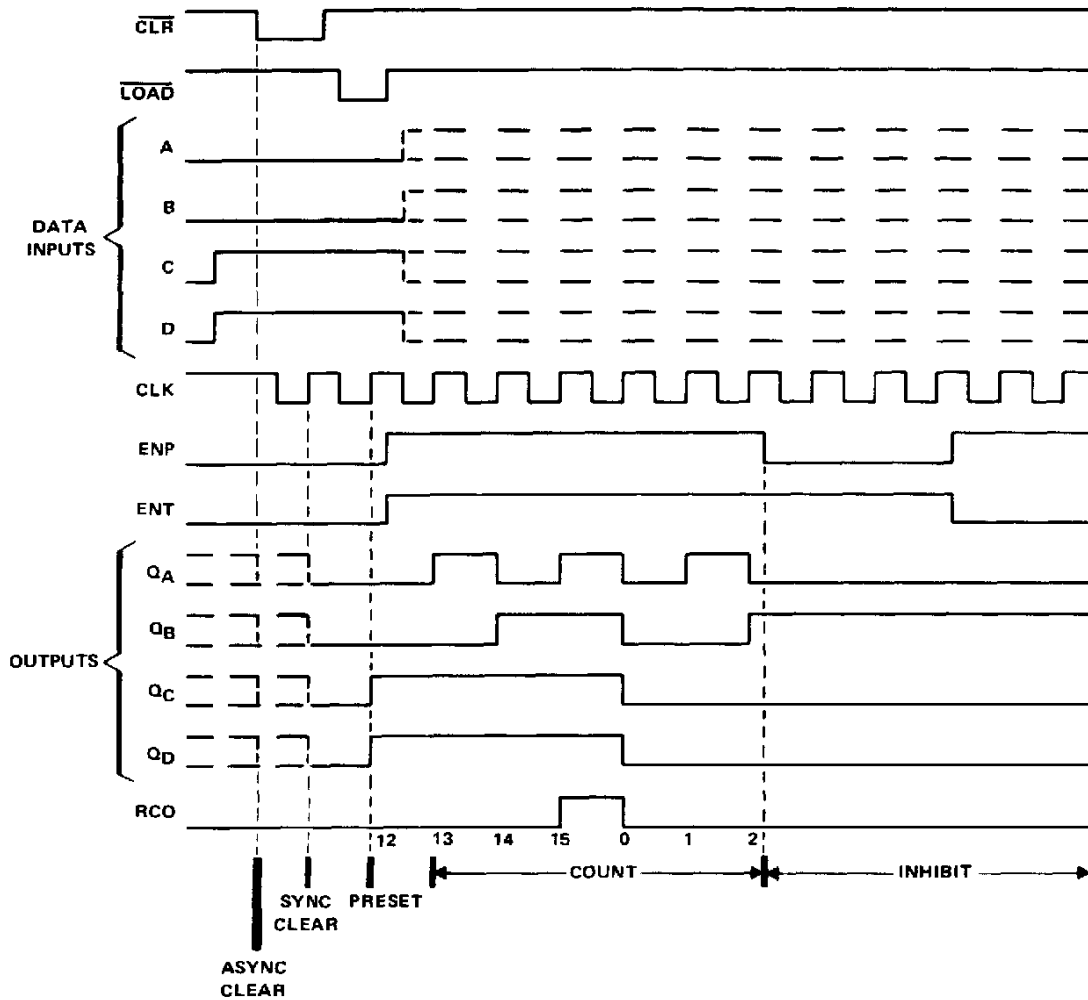


**SN54HC161, SN54HC163  
SN74HC160, SN74HC163  
SYNCHRONOUS 4-BIT BINARY COUNTERS**

**'HC161 and 'HC163 output sequence**

Illustrated below is the following sequence:

1. Clear outputs to zero (SN54HC161 and SN74HC161 are asynchronous; SN54HC163 and SN74HC163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, zero, one, and two
4. Inhibit



**SN54HC160 THRU SN54HC163  
SN74HC160 THRU SN74HC163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

**absolute maximum ratings over operating free-air temperature range†**

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND pins .....	$\pm 50$ mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package .....	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package .....	260°C
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54HC'			SN74HC'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5			V
		$V_{CC} = 4.5$ V	3.15		3.15			
		$V_{CC} = 6$ V	4.2		4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0	0.3	0	0.3	V	
		$V_{CC} = 4.5$ V	0	0.9	0	0.9		
		$V_{CC} = 6$ V	0	1.2	0	1.2		
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$t_t$	Input transition (rise and fall) times	$V_{CC} = 2$ V	0	1000	0	1000	ns	
		$V_{CC} = 4.5$ V	0	500	0	500		
		$V_{CC} = 6$ V	0	400	0	400		
$T_A$	Operating free-air temperature	-55		125	-40		85	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC'		SN74HC'		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	4.5 V	3.98	4.30		3.7		3.84			
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OH} = -4 \text{ mA}$	6 V	5.48	5.80		5.2		5.34		
		2 V		0.002	0.1		0.1		0.1	
		4.5 V		0.001	0.1		0.1		0.1	
	6 V		0.001	0.1		0.1		0.1		
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
		6 V		0.15	0.26		0.4		0.33	
$I_I$	$V_I = V_{CC}$ or 0	6 V		$\pm 0.1$	$\pm 100$		$\pm 1000$		$\pm 1000$	nA
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8		160		80	$\mu\text{A}$
$C_i$		2 to								pF
		6 V		3	10		10		10	





**SN54HC160 THRU SN54HC163  
SN74HC160 THRU SN74HC163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC160 THRU SN54HC163		SN74HC160 THRU SN74HC163		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t <sub>w</sub>	Pulse duration	CLK high or low	2 V	80	120	100	ns		
			4.5 V	16	24	20			
			6 V	14	20	17			
	$\overline{\text{CLR}}$ low ('HC160, 'HC161)	2 V	80	120	100				
		4.5 V	16	24	20				
		6 V	14	20	17				
t <sub>su</sub>	Setup time, before CLK†	A, B, C, or D	2 V	150	225	190	ns		
			4.5 V	30	45	38			
			6 V	26	38	32			
		$\overline{\text{LOAD}}$ low	2 V	135	205	170			
			4.5 V	27	41	34			
			6 V	23	35	29			
	ENP, ENT	2 V	170	255	215				
		4.5 V	34	51	43				
		6 V	29	43	37				
	$\overline{\text{CLR}}$ inactive ('HC160, 'HC161)	2 V	125	190	155				
		4.5 V	25	38	31				
		6 V	21	32	26				
	$\overline{\text{CLR}}$ low ('HC162, 'HC163)	2 V	160	240	200				
		4.5 V	32	48	40				
		6 V	27	41	34				
	$\overline{\text{CLR}}$ inactive ('HC162, 'HC163)	2 V	160	240	200				
		4.5 V	32	48	40				
		6 V	27	41	34				
t <sub>h</sub>	Hold time, all synchronous inputs after CLK†	2 V	0	0	0	ns			
		4.5 V	0	0	0				
		6 V	0	0	0				

**SN54HC160, SN54HC161  
SN74HC160, SN74HC161  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

switching characteristics over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 50$  pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC160 SN54HC161		SN74HC160 SN74HC161		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2 V	6	14		4.2		5	MHz	
			4.5 V	31	40		21		25		
			6 V	36	44		25		29		
t <sub>pd</sub>	CLK	RCO	2 V		83	215		325		270	ns
			4.5 V		24	43		65		54	
			6 V		20	37		55		46	
t <sub>pd</sub>	CLK	Any Q	2 V		80	205		310		255	ns
			4.5 V		25	41		62		51	
			6 V		21	35		53		43	
t <sub>pd</sub>	ENT	RCO	2 V		62	195		295		245	ns
			4.5 V		17	39		59		49	
			6 V		14	33		50		42	
t <sub>PHL</sub>	$\overline{CLR}$	Any Q	2 V		105	210		315		265	ns
			4.5 V		21	42		63		53	
			6 V		18	36		54		45	
t <sub>PHL</sub>	$\overline{CLR}$	RCO	2 V		110	220		330		275	ns
			4.5 V		22	44		66		55	
			6 V		19	37		56		47	
t <sub>t</sub>		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C <sub>pd</sub>	Power dissipation capacitance	No load, T <sub>A</sub> = 25°C	60 pF typ
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NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

**SN54HC162, SN54HC163**  
**SN74HC162, SN74HC163**  
**SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

switching characteristics over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 50$  pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC162 SN54HC163		SN74HC162 SN74HC163		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2 V	6	14		4.2		5	MHz	
			4.5 V	31	40		21		25		
			6 V	36	44		25		29		
t <sub>pd</sub>	CLK	RCO	2 V		83	215		325		270	ns
			4.5 V		24	43		65		54	
			6 V		20	37		55		46	
t <sub>pd</sub>	CLK	Any Q	2 V		80	205		310		255	ns
			4.5 V		25	41		62		51	
			6 V		21	35		53		43	
t <sub>pd</sub>	ENT	RCO	2 V		62	195		295		245	ns
			4.5 V		17	39		59		49	
			6 V		14	33		50		42	
t <sub>t</sub>		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C <sub>pd</sub>	Power dissipation capacitance	No load, T <sub>A</sub> = 25°C	60 pF typ
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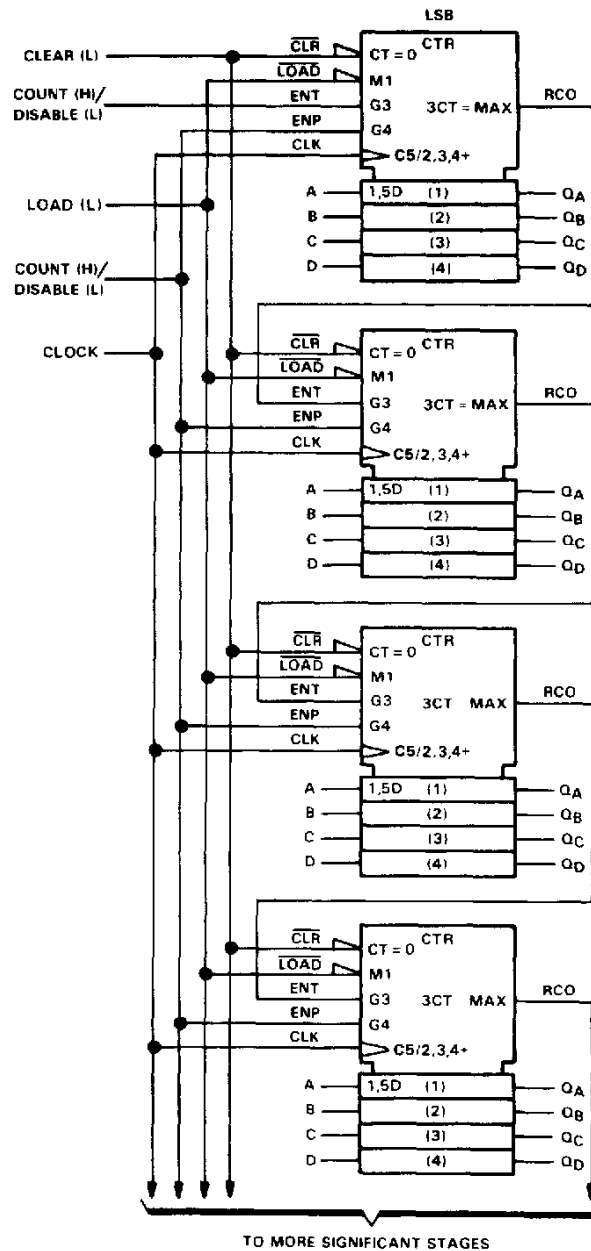
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

**SN54HC160 THRU SN54HC163  
SN74HC160 THRU SN74HC163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

**TYPICAL APPLICATION DATA**

**N-BIT SYNCHRONOUS COUNTERS**

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'HC160 and 'HC162 will count in BCD, and the 'HC161 and 'HC163 will count in binary. Virtually any count mode (modulo-N, N<sub>1</sub>-to-N<sub>2</sub>, N<sub>1</sub>-to-maximum) can be used with this fast look-ahead circuit.



**SN54HC160 THRU SN54HC163  
SN74HC160 THRU SN74HC163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

The application circuit shown on the preceding page is not valid for clock frequencies above 18 MHz (at 25°C and 4.5 V  $V_{CC}$ ). The reason for this is that there is a "glitch" that is produced on the second stage's RCO output and every succeeding stage's RCO output. This glitch is common to all HC vendors that Texas Instruments has evaluated in addition to the bipolar equivalents ('LS, 'ALS, 'AS).

The glitch on RCO is caused because the propagation delay of the rising edge of  $Q_A$  of the second stage is shorter than the propagation delay of the falling edge of ENT. The RCO output is the product of ENT,  $Q_A$ ,  $Q_B$ ,  $Q_C$ , and  $Q_D$  ( $ENT \cdot Q_A \cdot Q_B \cdot Q_C \cdot Q_D$ ). The resulting glitch is about 7-12 ns in duration. Figure 1 illustrates the condition in which the glitch occurs. For the purposes of simplicity, only two stages are being considered, but the results can be applied to other stages.  $Q_B$ ,  $Q_C$ , and  $Q_D$  of the first and second stage are at logic one, and  $Q_A$  of both stages are at logic zero (1110 1110) after the first clock pulse. On the rising edge of the second clock pulse,  $Q_A$  and RCO of the first stage will go high. On the rising edge of the third clock pulse  $Q_A$  and RCO of the first stage will return to a low level, and  $Q_A$  of the second stage will go to a high level. It is at this time that the glitch on the RCO of the second stage will appear because of the "race condition" inside the chip.

The glitch will cause a problem in the next stage (stage three) if the glitch is still present when the next rising clock edge appears (clock pulse 4). To ensure that this does not happen, the clock frequency must be less than inverse of the sum of the clock-to-RCO propagation delay and the glitch duration ( $t_g$ ). In other words,  $f_{max} = 1/(t_{pd} \text{ CLK-to-RCO} + t_g)$ . For example, at 25°C at 4.5 V  $V_{CC}$ , the clock-to-RCO propagation delay is 43 ns and the maximum duration of the glitch is 12 ns. Therefore, the maximum clock frequency that the cascaded counters can use is 18 MHz. The following table contains the  $f_{clock}$ ,  $t_w$ , and  $f_{max}$  specifications for applications that use more than two 'HC160 family devices cascaded together.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$		SN54HC160 thru SN54HC163		SN74HC160 thru SN74HC163		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
		$f_{clock}$ Clock frequency	2 V	0	3.6	0	2.5	
	4.5 V	0	18	0	12	0	14	
	6 V	0	21	0	14	0	17	
$t_w$ Pulse duration, CLK high or low	2 V	140		200		170		ns
	4.5 V	28		40		36		
	6 V	24		36		30		

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 50$  pF (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC160 thru SN54HC163		SN74HC160 thru SN74HC163		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
				$f_{max}$			2 V	3.6		2.5	
			4.5 V	18		12		14			
			6 V	21		14		17			

NOTE 1: These limits apply only to applications which use more than two 'HC160 family devices cascaded together.

**SN54HC160 THRU SN54HC163  
SN74HC160 THRU SN74HC163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

If the 'HC160 family is used as a single unit or only two cascaded together, then the maximum clock frequency that the devices can use is not limited because of the glitch. In these situations, the devices can be operated at the maximum specifications.

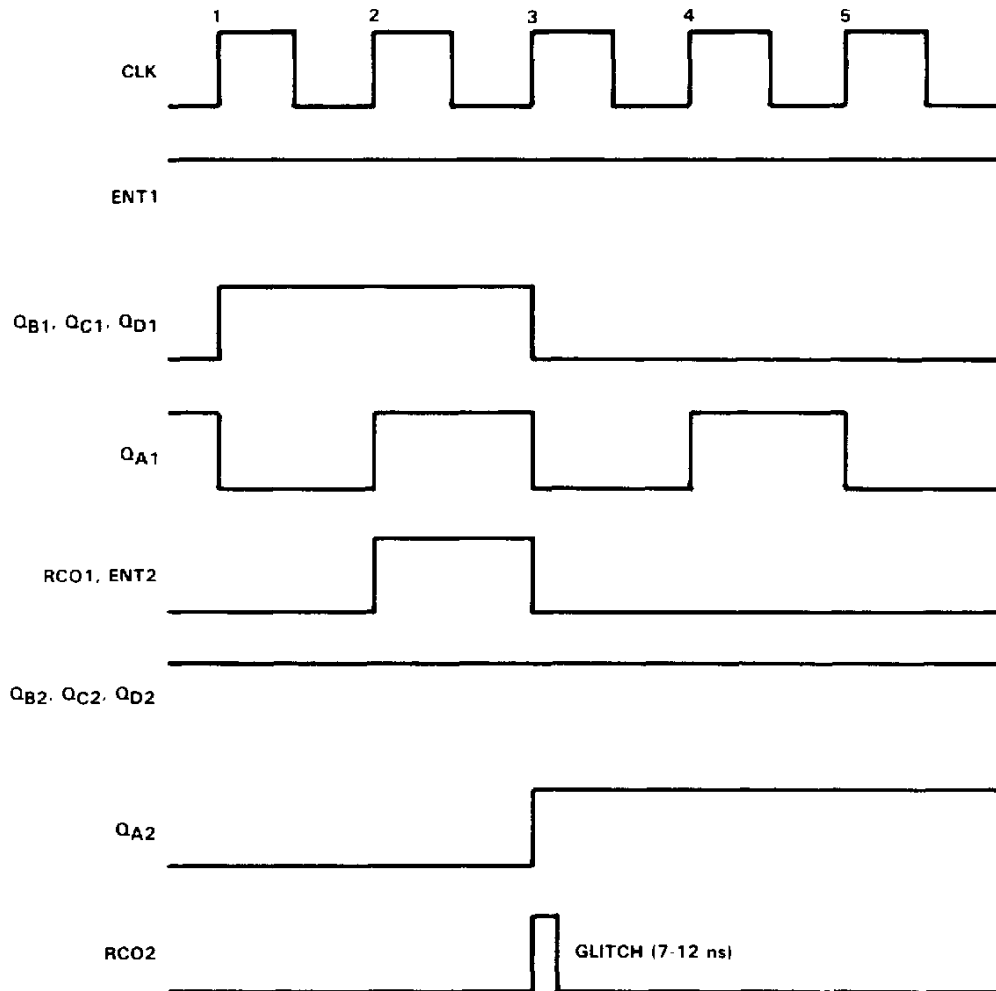


FIGURE 1

A glitch can appear on the RCO output of a single 'HC160 family device depending on the relationship of ENT to the clock input. Any application that uses the RCO output to drive any input except an ENT of another cascaded 'HC160 family device must take this into consideration.

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