

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT192

**Presettable synchronous BCD
decade up/down counter**

Product specification
File under Integrated Circuits, IC06

December 1990

Presettable synchronous BCD decade up/down counter

74HC/HCT192

FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT192 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT192 are synchronous BCD up/down counters. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up. If the CP_D clock is pulsed while CP_U is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input (\overline{PL}).

The "192" contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up (\overline{TC}_U) and terminal count down (\overline{TC}_D) outputs are normally HIGH. When the circuit has reached the maximum count state of 9, the next HIGH-to-LOW transition of CP_U will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again, duplicating the count up clock.

Likewise, the \overline{TC}_D output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D₀ to D₃) is loaded into the counter and appears on the outputs (Q₀ to Q₃) regardless of the conditions of the clock inputs when the parallel load (\overline{PL}) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q₀ to Q₃) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

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QUICK REFERENCE DATAGND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------|---|---|---------|-----|------|
| | | | HC | HCT | |
| t_{PHL}/t_{PLH} | propagation delay CP_D, CP_U to Q_n | $C_L = 15\text{ pF}; V_{CC} = 5\text{ V}$ | 20 | 20 | ns |
| f_{max} | maximum clock frequency | | 40 | 45 | MHz |
| C_I | input capacitance | | 3.5 | 3.5 | pF |
| C_{PD} | power dissipation capacitance per package | notes 1 and 2 | 24 | 28 | pF |

Notes

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

- For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

Pre-settable synchronous BCD decade up/down counter

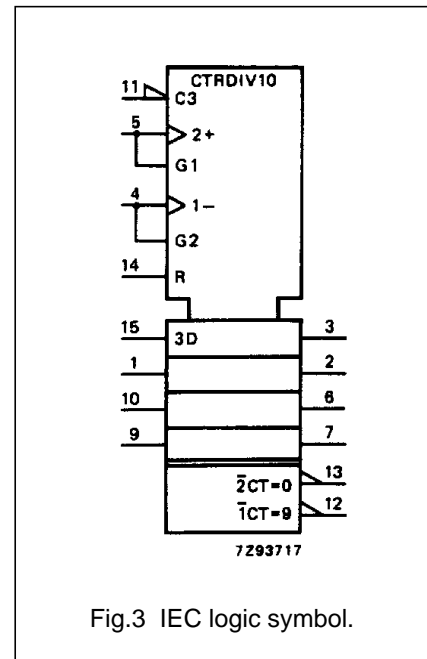
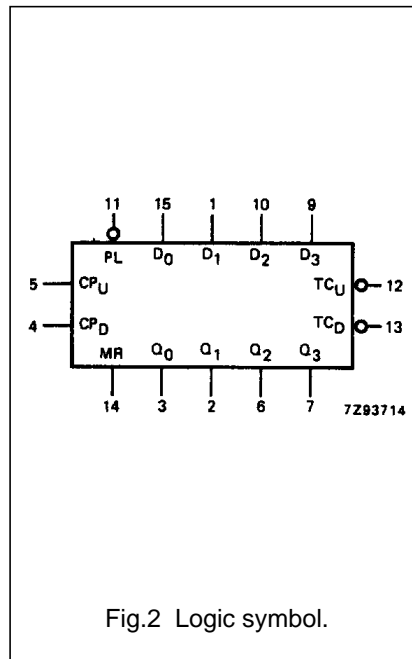
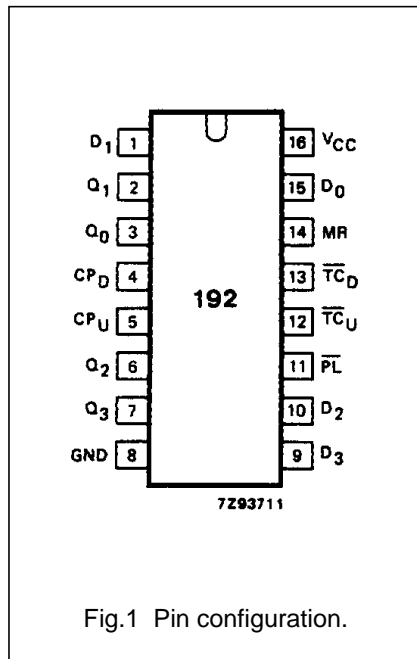
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PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|--------------|-----------------------------------|--|
| 3, 2, 6, 7 | Q ₀ to Q ₃ | flip-flop outputs |
| 4 | CP _D | count down clock input ⁽¹⁾ |
| 5 | CP _U | count up clock input ⁽¹⁾ |
| 8 | GND | ground (0 V) |
| 11 | $\overline{\text{PL}}$ | asynchronous parallel load input (active LOW) |
| 12 | $\overline{\text{TC}}_{\text{U}}$ | terminal count up (carry) output (active LOW) |
| 13 | $\overline{\text{TC}}_{\text{D}}$ | terminal count down (borrow) output (active LOW) |
| 14 | MR | asynchronous master reset input (active HIGH) |
| 15, 1, 10, 9 | D ₀ to D ₃ | data inputs |
| 16 | V _{CC} | positive supply voltage |

Note

1. LOW-to-HIGH, edge triggered



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FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | | | | OUTPUTS | | | | | |
|----------------|--------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|---------------------------------|----------------|----------------|------------------|-------------------|-------------------|
| | MR | \overline{PL} | CP _U | CP _D | D ₀ | D ₁ | D ₂ | D ₃ | Q ₀ | Q ₁ | Q ₂ | Q ₃ | \overline{TC}_U | \overline{TC}_D |
| reset (clear) | H | X | X | L | X | X | X | X | L | L | L | L | H | L |
| | H | X | X | H | X | X | X | X | L | L | L | L | H | H |
| parallel load | L | L | X | L | L | L | L | L | L | L | L | L | H | L |
| | L | L | X | H | L | L | L | L | L | L | L | L | H | H |
| | L | L | L | X | H | X | X | H | Q _n = D _n | | | L | H | |
| | L | L | H | X | H | X | X | H | Q _n = D _n | | | H | H | |
| count up | L | H | ↑ | H | X | X | X | X | count up | | | H ⁽²⁾ | H | |
| count down | L | H | H | ↑ | X | X | X | X | count down | | | H | H ⁽³⁾ | |

Notes

- H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
- \overline{TC}_U = CP_U at terminal count up (HLLH)
- \overline{TC}_D = CP_D at terminal count down (LLLL)

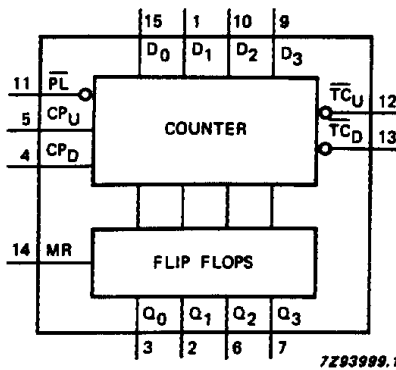


Fig.4 Functional diagram.

Pre-settable synchronous BCD decade up/down counter

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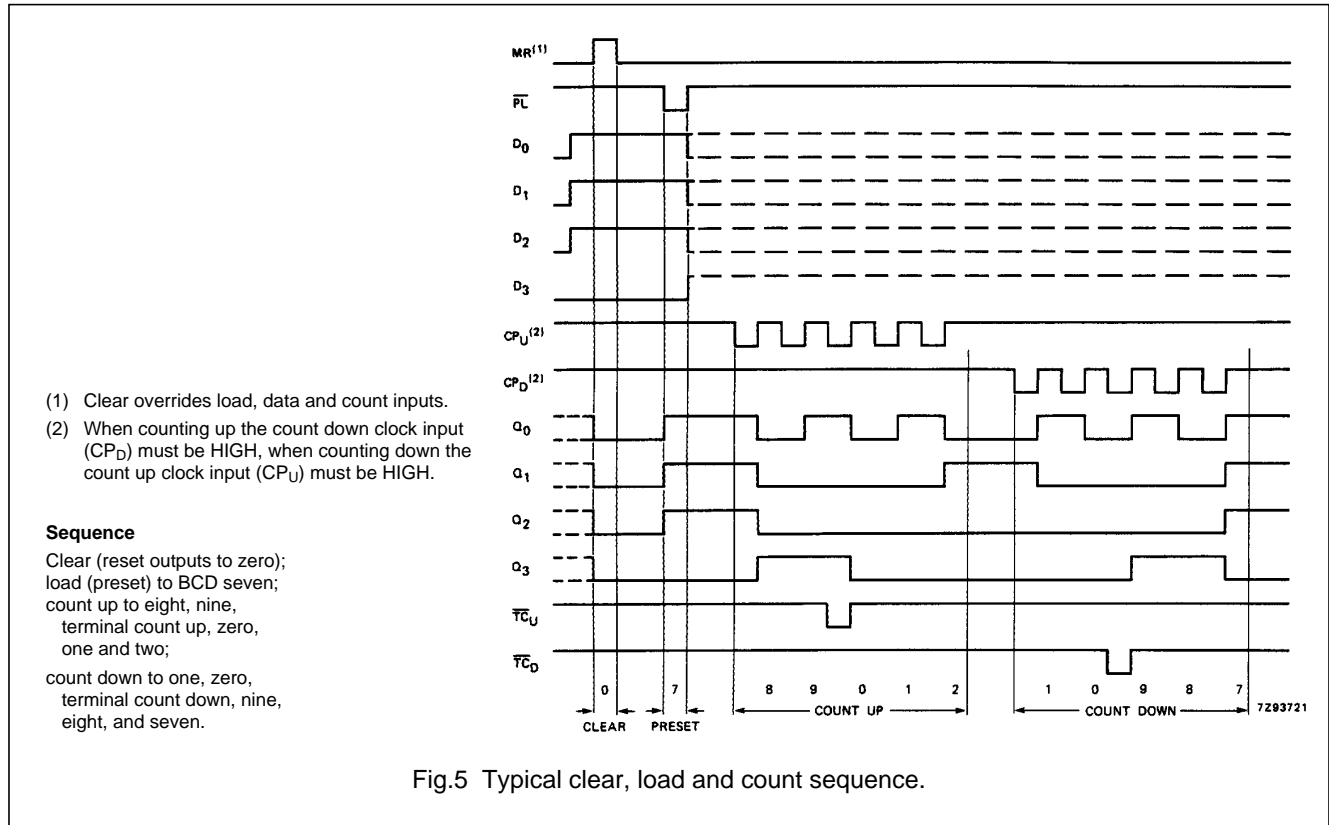


Fig.5 Typical clear, load and count sequence.

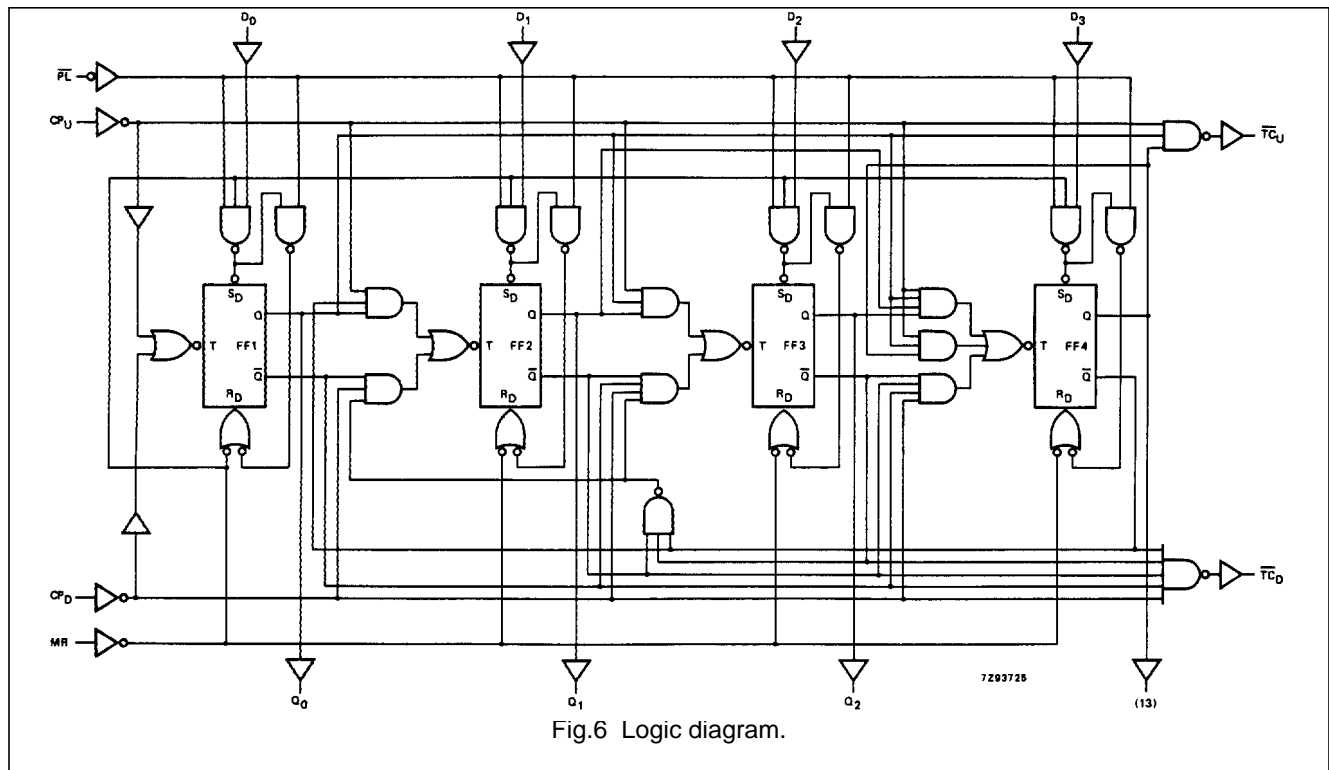


Fig.6 Logic diagram.

Presettable synchronous BCD decade up/down counter

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|---|-----------------------|-----------------|-----------------|------------|-----------------|-------------|-----------------|------------------------|-------------------|--------|
| | | 74HC | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay CP _U , CP _D to Q _n | | 66 24 19 | 215 43 37 | | 270 54 46 | | 325 65 55 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{PHL} / t _{PLH} | propagation delay CP _U to TC _U | | 33 12 10 | 125 25 21 | | 155 31 26 | | 190 38 32 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{PHL} / t _{PLH} | propagation delay CP _D to TC _D | | 39 14 11 | 125 25 21 | | 155 31 26 | | 190 38 32 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{PHL} / t _{PLH} | propagation delay PL to Q _n | | 69 25 20 | 215 43 37 | | 270 54 46 | | 325 65 55 | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{PHL} | propagation delay MR to Q _n | | 63 23 18 | 200 40 34 | | 250 50 43 | | 300 60 51 | ns | 2.0 4.5 6.0 | Fig.10 |
| t _{PHL} | propagation delay D _n to Q _n | | 91 33 26 | 275 55 47 | | 345 69 59 | | 415 83 71 | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{PLH} | propagation delay D _n to Q _n | | 80 29 23 | 240 48 41 | | 300 60 51 | | 360 72 61 | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{PHL} / t _{PLH} | propagation delay PL to \overline{TC}_U , PL to \overline{TC}_D | | 102 37 30 | 315 63 54 | | 395 79 67 | | 475 95 81 | ns | 2.0 4.5 6.0 | Fig.12 |
| t _{PHL} / t _{PLH} | propagation delay MR to \overline{TC}_U , MR to \overline{TC}_D | | 96 35 28 | 285 57 48 | | 355 71 60 | | 430 86 73 | ns | 2.0 4.5 6.0 | Fig.12 |
| t _{PHL} / t _{PLH} | propagation delay D _n to \overline{TC}_U , D _n to \overline{TC}_D | | 83 30 24 | 290 58 49 | | 365 73 62 | | 435 87 74 | ns | 2.0 4.5 6.0 | Fig.12 |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | Fig.10 |

Pre-settable synchronous BCD decade up/down counter

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| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|------------------|---|-----------------------|-----------------|------|-----------------|------|-----------------|------|------|------------------------|---|
| | | 74HC | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _w | up clock pulse width HIGH or LOW | 120 24 20 | 39 14 11 | | 150 30 26 | | 180 36 31 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _w | down clock pulse width HIGH or LOW | 140 28 24 | 50 18 14 | | 175 35 30 | | 210 42 36 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _w | master reset pulse width HIGH | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.10 |
| t _w | parallel load pulse width LOW | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{rem} | removal time \overline{PL} to CP _U , CP _D | 50 10 9 | 3 1 1 | | 65 13 11 | | 75 15 13 | | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{rem} | removal time MR to CP _U , CP _D | 50 10 9 | 0 0 0 | | 65 13 11 | | 75 15 13 | | ns | 2.0 4.5 6.0 | Fig.10 |
| t _{su} | set-up time D _n to \overline{PL} | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.11 note: CP _U = CP _D = HIGH |
| t _h | hold time D _n to \overline{PL} | 0 0 0 | -14 -5 -4 | | 0 0 0 | | 0 0 0 | | ns | 2.0 4.5 6.0 | Fig.11 |
| t _h | hold time CP _U to CP _D , CP _D to CP _U | 80 16 14 | 19 7 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.13 |
| f _{max} | maximum up, down clock pulse frequency | 4.0 20 24 | 12 36 43 | | 3.2 16 19 | | 2.6 13 15 | | MHz | 2.0 4.5 6.0 | Fig.7 |

**Presettable synchronous BCD decade
up/down counter**

74HC/HCT192**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-----------------------------------|------------------------------|
| D _n | 0.35 |
| CP _U , CP _D | 1.40 |
| \overline{PL} | 0.65 |
| MR | 1.05 |

Presettable synchronous BCD decade up/down counter

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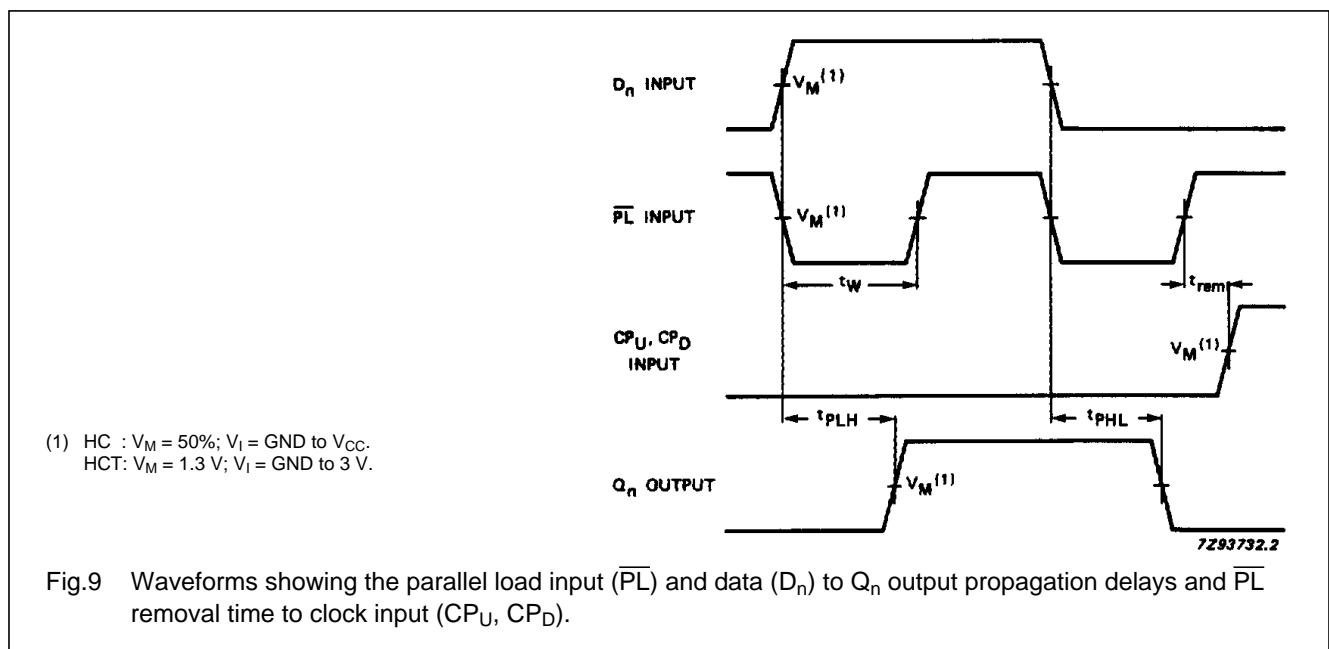
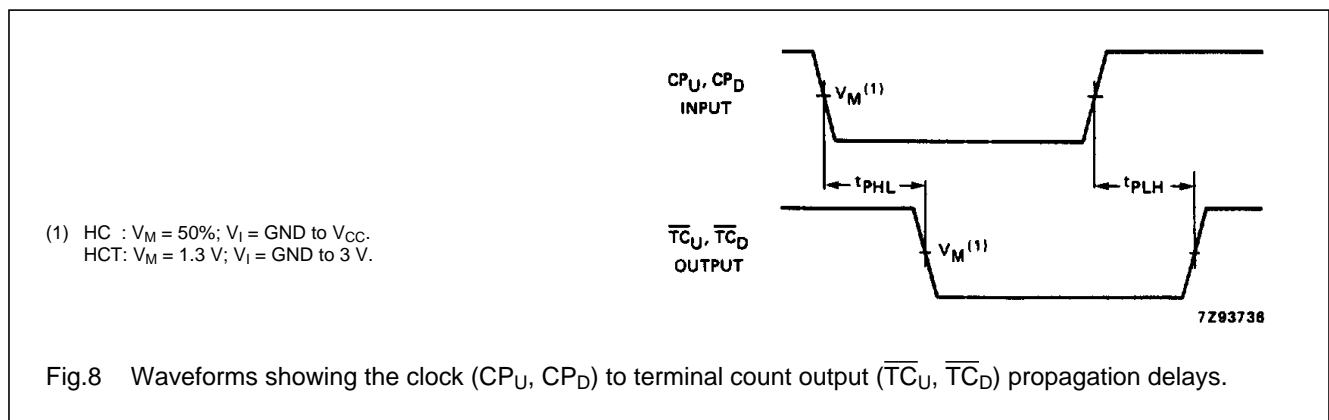
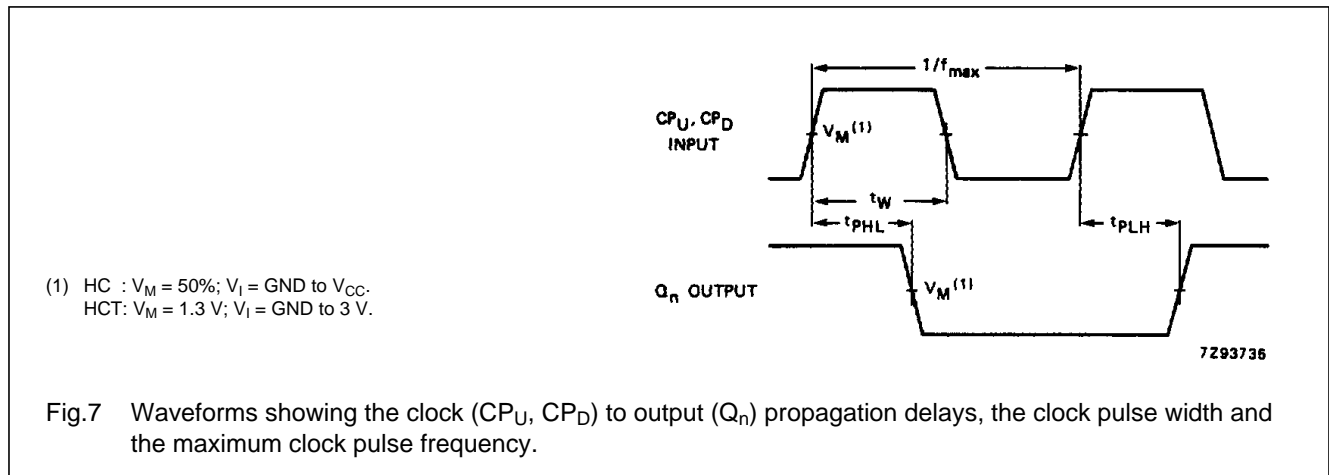
AC CHARACTERISTICS FOR 74HCTGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|--|-----------------------|------|------|------------|------|-------------|------|-----|------|---|-----------|
| | | 74HCT | | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t _{PHL} / t _{PLH} | propagation delay CP _U , CP _D to Q _n | | 23 | 43 | | 54 | | 65 | ns | 4.5 | Fig.7 | |
| t _{PHL} / t _{PLH} | propagation delay CP _U to \overline{TC}_U | | 16 | 30 | | 38 | | 45 | ns | 4.5 | Fig.8 | |
| t _{PHL} / t _{PLH} | propagation delay CP _D to \overline{TC}_D | | 17 | 30 | | 38 | | 45 | ns | 4.5 | Fig.8 | |
| t _{PHL} / t _{PLH} | propagation delay PL to Q _n | | 28 | 46 | | 58 | | 69 | ns | 4.5 | Fig.9 | |
| t _{PHL} | propagation delay MR to Q _n | | 24 | 40 | | 50 | | 60 | ns | 4.5 | Fig.10 | |
| t _{PHL} / t _{PLH} | propagation delay D _n to Q _n | | 36 | 62 | | 78 | | 93 | ns | 4.5 | Fig.9 | |
| t _{PHL} / t _{PLH} | propagation delay PL to \overline{TC}_U , PL to \overline{TC}_D | | 36 | 64 | | 80 | | 96 | ns | 4.5 | Fig.12 | |
| t _{PHL} / t _{PLH} | propagation delay MR to \overline{TC}_U , MR to \overline{TC}_D | | 36 | 64 | | 80 | | 96 | ns | 4.5 | Fig.12 | |
| t _{PHL} / t _{PLH} | propagation delay D _n to \overline{TC}_U , D _n to \overline{TC}_D | | 33 | 58 | | 73 | | 87 | ns | 4.5 | Fig.12 | |
| t _{THL} / t _{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.10 | |
| t _w | up, down clock pulse width HIGH or LOW | 25 | 14 | | 31 | | 38 | | ns | 4.5 | Fig.7 | |
| t _w | master reset pulse width HIGH | 16 | 6 | | 20 | | 24 | | ns | 4.5 | Fig.10 | |
| t _w | parallel load pulse width LOW | 20 | 10 | | 25 | | 30 | | ns | 4.5 | Fig.9 | |
| t _{rem} | removal time PL to CP _U , CP _D | 10 | 1 | | 13 | | 15 | | ns | 4.5 | Fig.9 | |
| t _{rem} | removal time MR to CP _U , CP _D | 10 | 2 | | 13 | | 15 | | ns | 4.5 | Fig.10 | |
| t _{su} | set-up time D _n to PL | 16 | 8 | | 20 | | 24 | | ns | 4.5 | Fig.11 note: CP _U = CP _D = HIGH | |
| t _h | hold time D _n to PL | 0 | -6 | | 0 | | 0 | | ns | 4.5 | Fig.11 | |
| t _h | hold time CP _U to CP _D , CP _D to CP _U | 20 | 9 | | 25 | | 30 | | ns | 4.5 | Fig.13 | |
| f _{max} | maximum up, down clock pulse frequency | 20 | 41 | | 16 | | 13 | | MHz | 4.5 | Fig.7 | |

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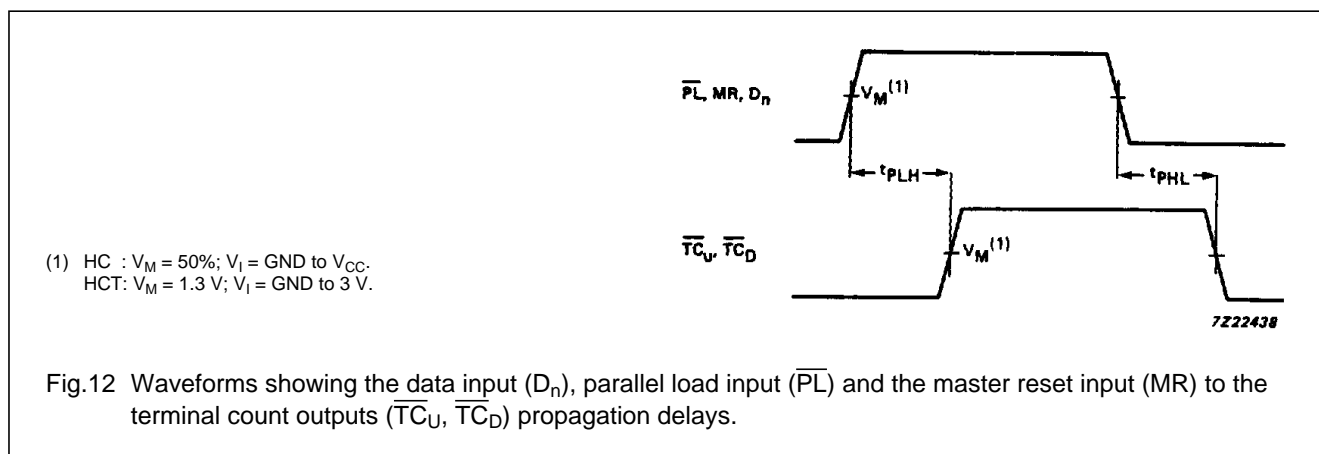
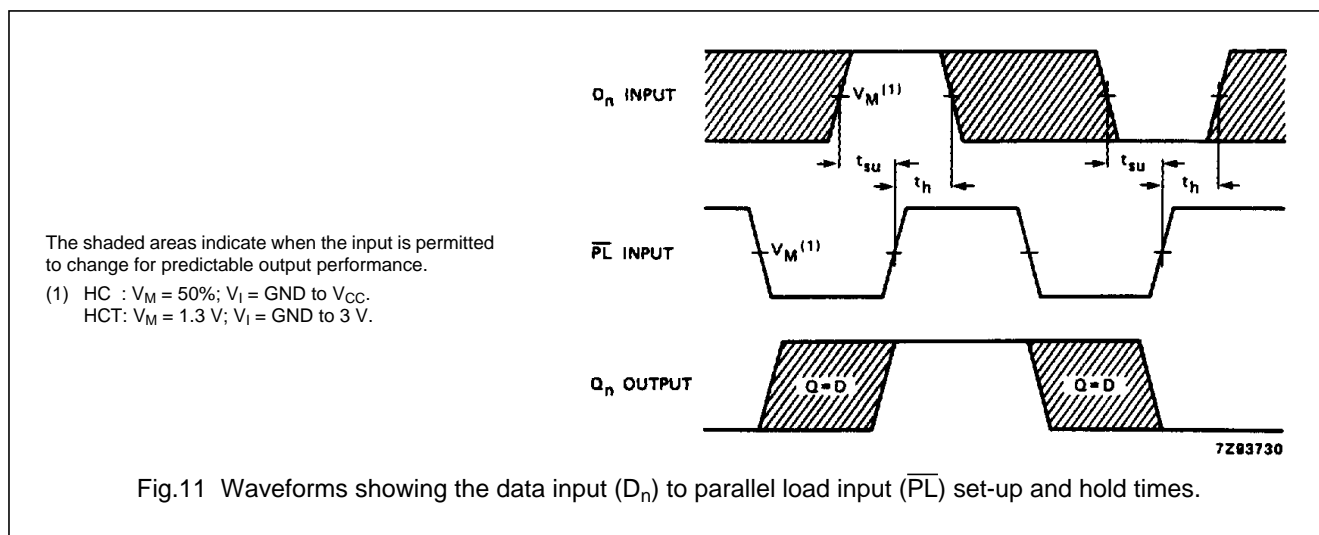
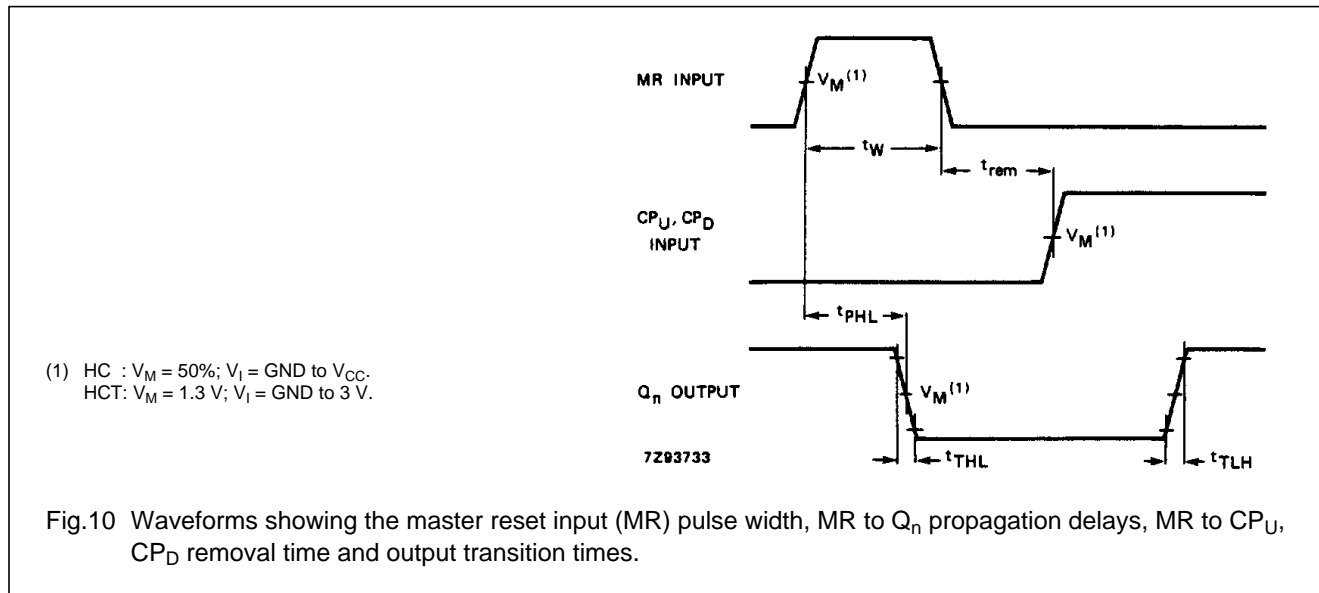
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AC WAVEFORMS



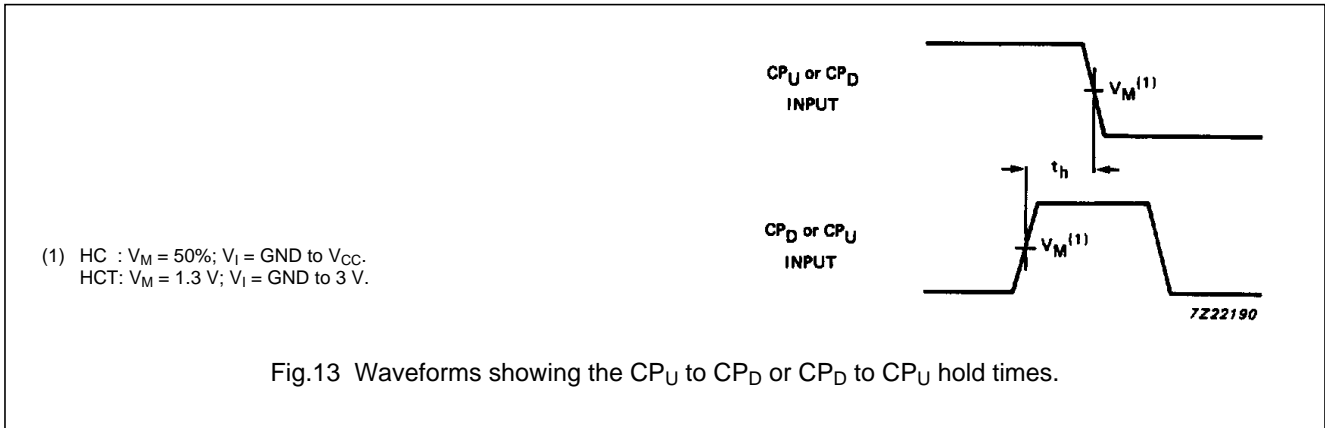
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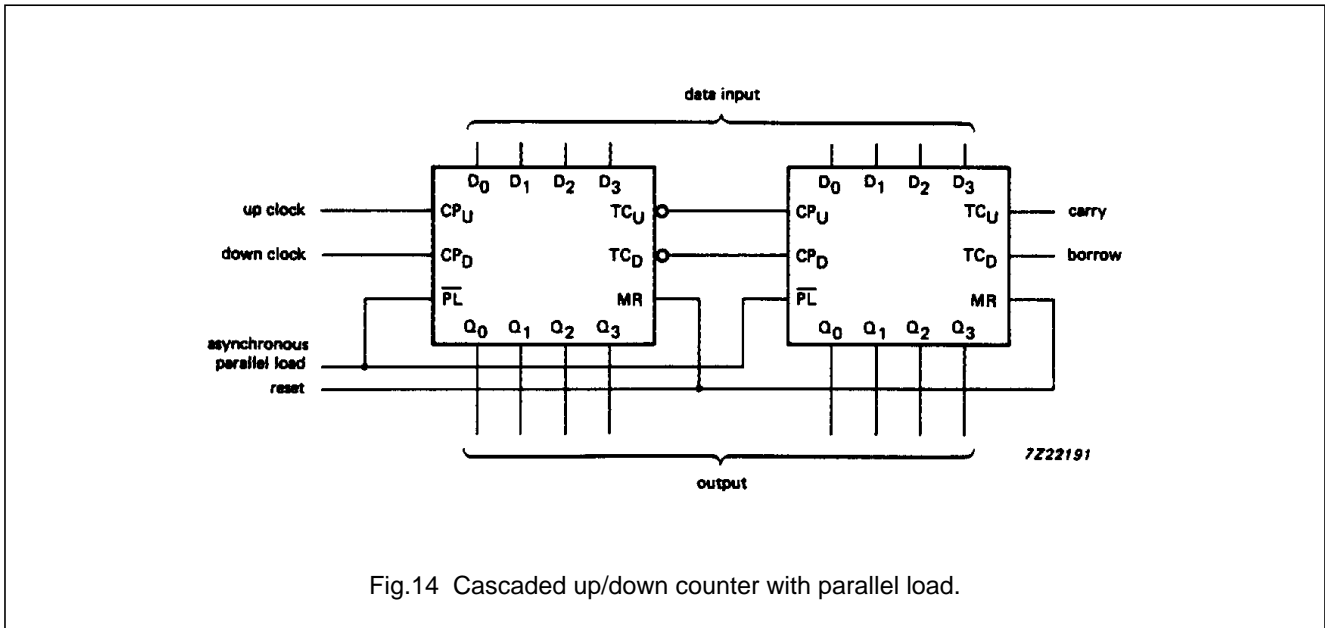


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APPLICATION INFORMATION



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".