

# HM628512 Series

524288-word  $\times$  8-bit High Speed CMOS Static RAM

# HITACHI

Rev. 5.0  
Nov. 23, 1994

The Hitachi HM628512 is a 4M-bit static RAM organized 524288-word  $\times$  8-bit. It realizes higher density, higher performance and low power consumption by employing 0.5  $\mu\text{m}$  Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. LP-version is suitable for battery back up system.

## Features

- High speed: Fast access time:
  - 55/70/85/100 ns (max)
- Low power
  - Standby: 10  $\mu\text{W}$  (typ) (L/L-SL version)
  - Operation: 75 mW (typ) (f=1MHz)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L/L-SL version)

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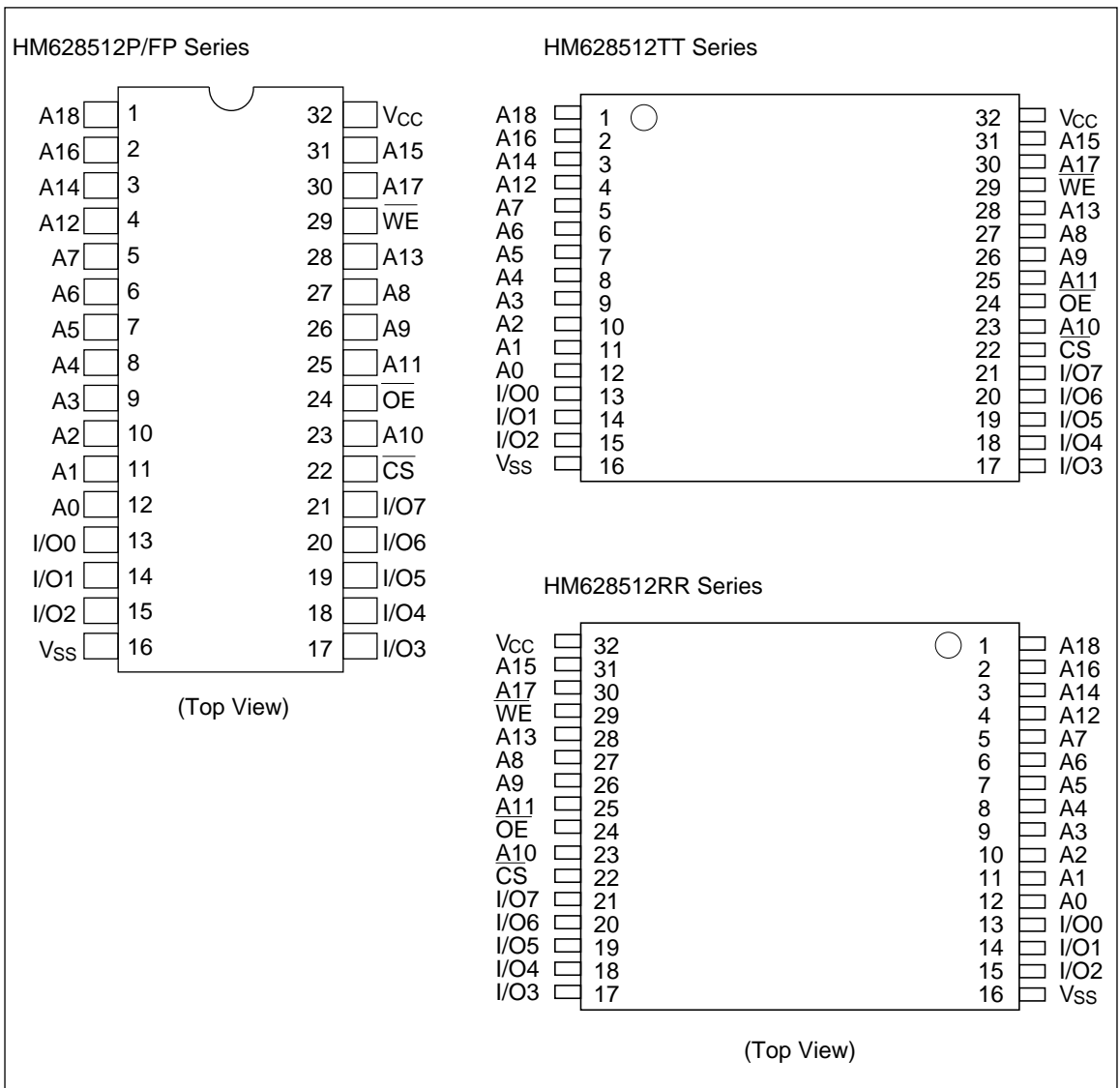
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### Ordering Information

Type No.	Access time	Package	Type No.	Access time	Package
HM628512P-5	55 ns	600-mil 32-pin plastic DIP (DP-32)	HM628512LTT-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512P-7	70 ns				
HM628512P-8	85 ns				
HM628512P-10	100 ns				
HM628512LP-5	55 ns		HM628512LTT-5SL	55 ns	
HM628512LP-7	70 ns				
HM628512LP-8	85 ns				
HM628512LP-10	100 ns				
HM628512LFP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)	HM628512LRR-5	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512LFP-7	70 ns				
HM628512LFP-8	85 ns				
HM628512LFP-10	100 ns				
HM628512LFP-5	55 ns		HM628512LRR-5SL	55 ns	
HM628512LFP-7	70 ns				
HM628512LFP-8	85 ns				
HM628512LFP-10	100 ns				
HM628512LFP-5SL	55 ns		HM628512LRR-7SL	70 ns	
HM628512LFP-7SL	70 ns				
HM628512LFP-8SL	85 ns				
HM628512LFP-10SL	100 ns				
			HM628512LRR-8SL	85 ns	
			HM628512LRR-10SL	100 ns	

**Pin Arrangement**

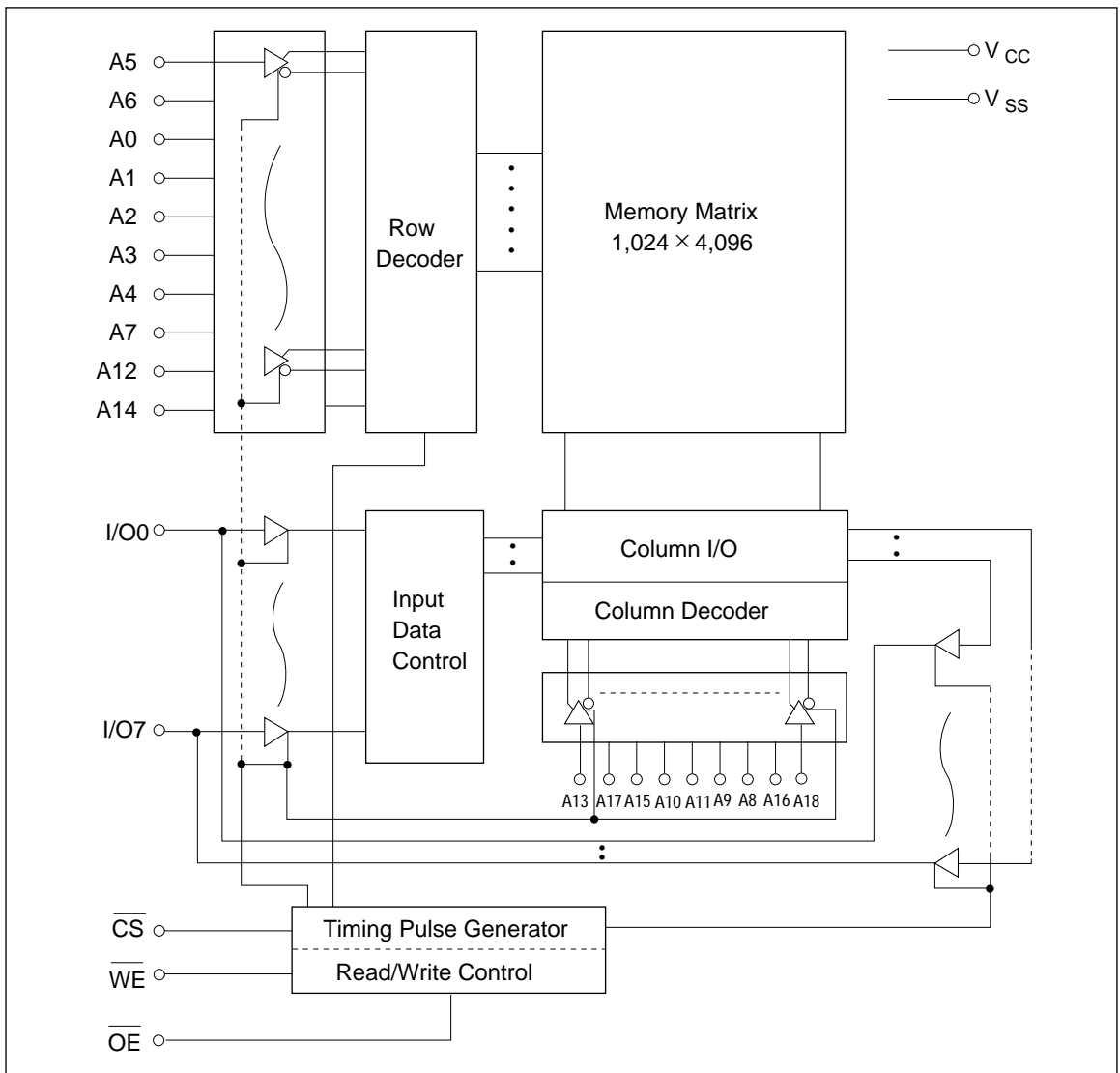


**Pin Description**

Symbol	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
CS	Chip select
WE	Write enable
OE	Output enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

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## Block Diagram



**Function Table**

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	$V_{CC}$ current	Dout pin	Ref. cycle
X	H	X	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	Output disable	$I_{CC}$	High-Z	—
H	L	L	Read	$I_{CC}$	Dout	Read cycle
L	L	H	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: X: H or L

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 <sup>*1</sup> to +7.0	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-10 to +85	°C

Note: 1. -3.0 V for pulse half-width ≤ 30 ns

**Recommended DC Operating Conditions ( $T_a = 0$  to +70°C)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input high (logic 1) voltage	$V_{IH}$	2.2	—	6.0	V
Input low (logic 0) voltage	$V_{IL}$	-0.3 <sup>*1</sup>	—	0.8	V

Note: 1. -3.0 V for pulse half-width ≤ 30 ns

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### DC Characteristics (Ta = 0 to +70°C, VCC = 5 V ±10% , VSS = 0 V)

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions	
Input leakage current	I <sub>LI</sub>	—	—	1	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Output leakage current	I <sub>LO</sub>	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Operating power supply current: DC	I <sub>CC READ</sub>	—	15	25	mA	$\overline{CS} = V_{IL}$ , $\overline{WE} = V_{IH}$ others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA	
	I <sub>CC WRITE</sub>	—	20	45	mA	$\overline{CS} = V_{IL}$ , $\overline{WE} = V_{IL}$ others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA	
Operating power supply current	-5	I <sub>CC1</sub>	—	70	100	mA	Min cycle, duty = 100%
	-7	I <sub>CC1</sub>	—	60	90	mA	$\overline{CS} = V_{IL}$ , others = V <sub>IH</sub> /V <sub>IL</sub>
	-8/10	I <sub>CC1</sub>	—	55	80	mA	I <sub>I/O</sub> = 0 mA
		I <sub>CC2</sub>	—	15	30	mA	Cycle time = 1 μs, duty = 100% I <sub>I/O</sub> = 0 mA, $\overline{CS} \leq 0.2$ V V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IL</sub> ≤ 0.2 V
Standby power supply current: DC	I <sub>SB</sub>	—	1	3	mA	$\overline{CS} = V_{IH}$	
Standby power supply current (1): DC	I <sub>SB1</sub>	—	0.02	2	mA	V <sub>in</sub> ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V	
		—	2	100* <sup>2</sup>	μA		
		—	2	50* <sup>3</sup>	μA		
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.1 mA	
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1.0 mA	

- Notes: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.  
 2. This characteristics is guaranteed only for L version.  
 3. This characteristics is guaranteed only for L-SL version.

### Capacitance (Ta = 25°C, f = 1 MHz)\*<sup>1</sup>

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	C <sub>in</sub>	—	8	pF	V <sub>in</sub> = 0 V
Input/output capacitance	C <sub>I/O</sub>	—	10	pF	V <sub>I/O</sub> = 0 V

- Note: 1. This parameter is sampled and not 100% tested.

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ , unless otherwise noted.)

**Test Conditions**

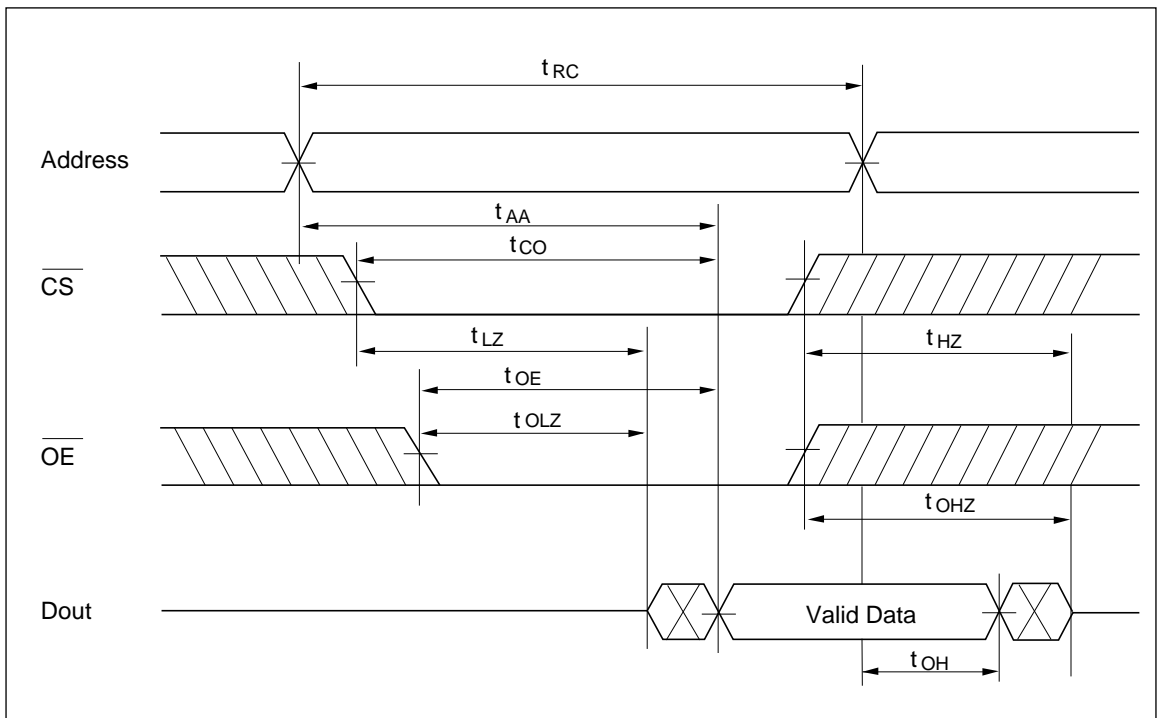
- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate +  $C_L$  (100 pF)  
(HM628512-7/8/10)  
1 TTL Gate +  $C_L$  (50 pF)  
(HM628512-5)  
(Including scope & jig)

**Read Cycle**

		HM628512									
		-5		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Read cycle time	$t_{RC}$	55	—	70	—	85	—	100	—	ns	
Address access time	$t_{AA}$	—	55	—	70	—	85	—	100	ns	
Chip select access time	$t_{CO}$	—	55	—	70	—	85	—	100	ns	
Output enable to output valid	$t_{OE}$	—	25	—	35	—	45	—	50	ns	
Chip selection to output in low-Z	$t_{LZ}$	10	—	10	—	10	—	10	—	ns	2, 3
Output enable to output in low-Z	$t_{OLZ}$	5	—	5	—	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	$t_{HZ}$	0	20	0	25	0	30	0	35	ns	1, 2, 3
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	0	30	0	35	ns	1, 2, 3
Output hold from address change	$t_{OH}$	10	—	10	—	10	—	10	—	ns	

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## Read Timing Waveform\*4



- Notes:
1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. At any given temperature and voltage condition,  $t_{HZ}$  (max) is less than  $t_{LZ}$  (min).
  3. This parameter is sampled and not 100% tested.
  4.  $\overline{WE}$  is high for read cycle.

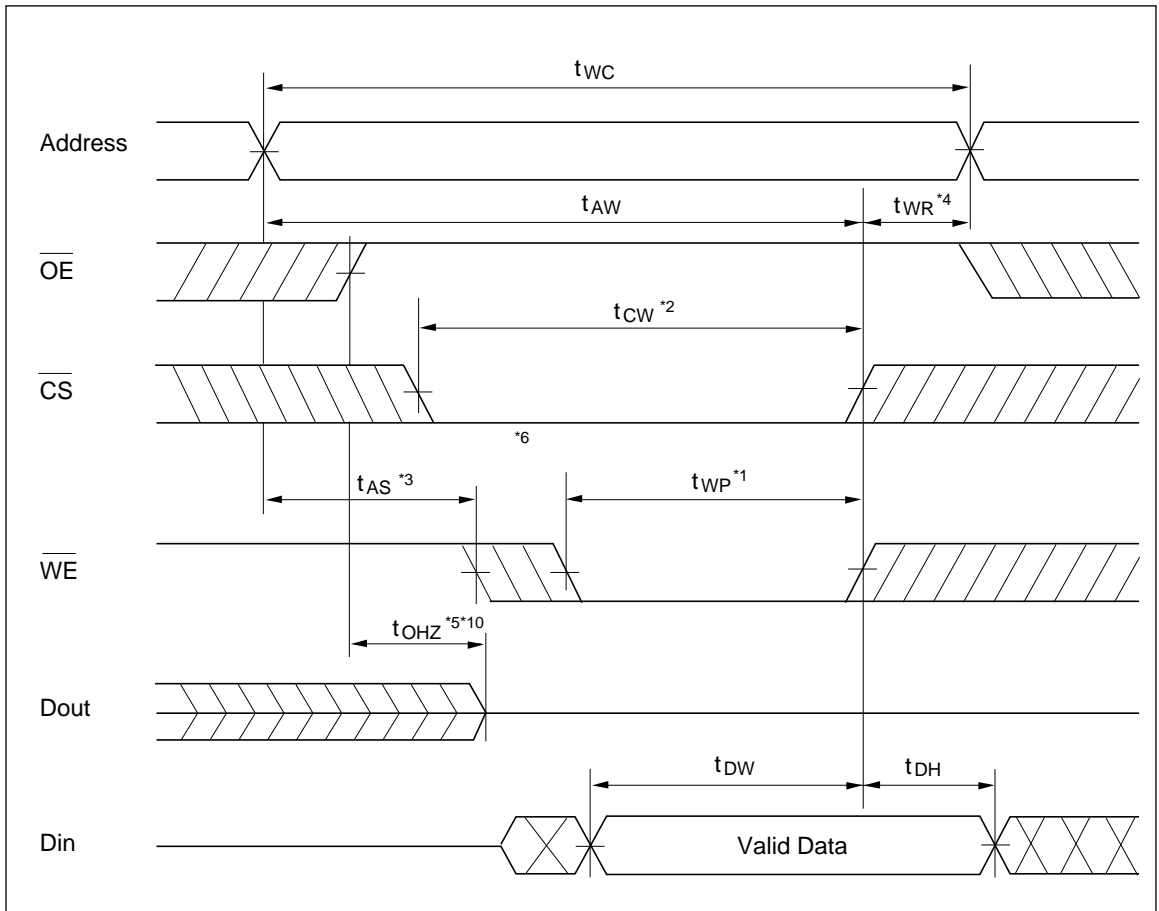


Write Cycle

Parameter	Symbol	HM628512								Unit	Note
		-5		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	55	—	70	—	85	—	100	—	ns	
Chip selection to end of write	$t_{CW}$	50	—	60	—	75	—	80	—	ns	2
Address setup time	$t_{AS}$	0	—	0	—	0	—	0	—	ns	3
Address valid to end of write	$t_{AW}$	50	—	60	—	75	—	80	—	ns	
Write pulse width	$t_{WP}$	40	—	50	—	55	—	60	—	ns	1, 12
Write recovery time	$t_{WR}$	5	—	5	—	5	—	5	—	ns	4
$\overline{WE}$ to output in high-Z	$t_{WHZ}$	0	20	0	25	0	30	0	35	ns	10, 11
Data to write time overlap	$t_{DW}$	25	—	30	—	35	—	40	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	5	—	5	—	ns	10

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## Write Timing Waveform (1) ( $\overline{\text{OE}}$ Clock)





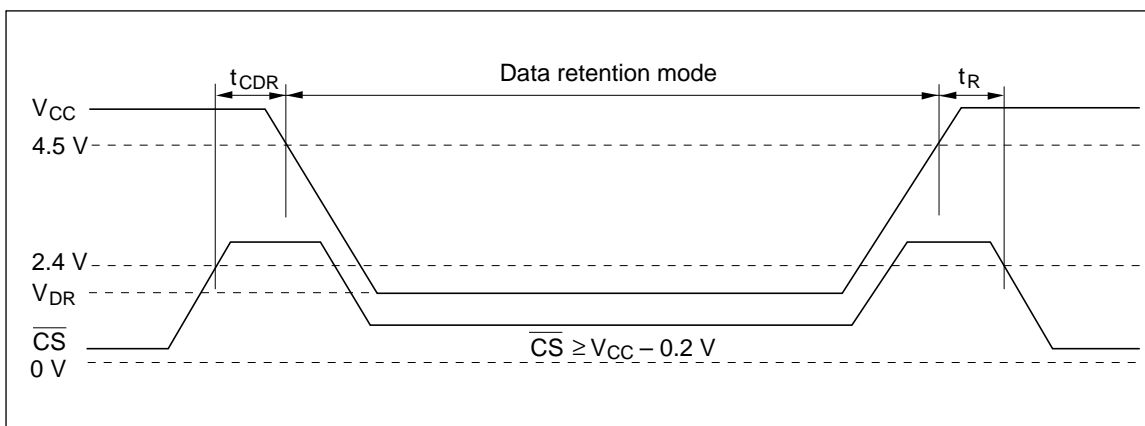
## HM628512 Series

### Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $+70^\circ\text{C}$ )

This characteristics is guaranteed only for L/L-SL version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*3
$V_{CC}$ for data retention	$V_{DR}$	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{in} \geq 0$ V
Data retention current	$I_{CCDR}$	—	1*4	50*1	$\mu\text{A}$	$V_{CC} = 3.0$ V, $V_{in} \geq 0$ V
		—	1*4	15*2	$\mu\text{A}$	$\overline{CS} \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	5	—	—	ms	

### Low $V_{CC}$ Data Retention Timing Waveform ( $\overline{CS}$ Controlled)



- Notes:
1. For L-version and 20  $\mu\text{A}$  (max.) at  $T_a = 0$  to  $40^\circ\text{C}$ .
  2. For SL-version and 3  $\mu\text{A}$  (max.) at  $T_a = 0$  to  $40^\circ\text{C}$ .
  3.  $\overline{CS}$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{OE}$  buffer, and  $D_{in}$  buffer. In data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.
  4. Typical values are at  $V_{CC} = 3.0$  V,  $T_a = 25^\circ\text{C}$  and specified loading, and not guaranteed.