SRM20100LC70/85/10

CMOS 1M-BIT STATIC RAM

- **Low Supply Current**
- **Access Time 70ns/85ns/100ns**
- **131,072 Words×8-Bit Asynchronous**

■DESCRIPTION

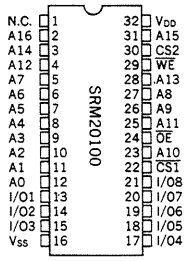
The SRM20100LC70/85/10 is an 131,072 words×8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

■FEATURES

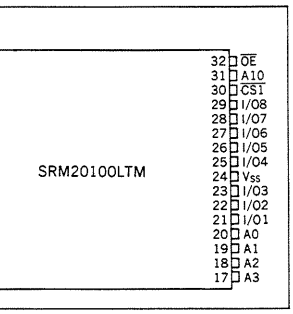
- Fast Access time ····· SRM20100LC70 70ns (Max)*
  SRM20100LC85 85ns (Max)
  SRM20100LC10 100ns (Max)
- Low supply current ····· standby : 2μA (Typ)
  operation: 15mA/MHz (Typ)
- Completely static ····· No clock required
- Single power supply ····· 5V±10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package ····· SRM20100LC70/85/10 DIP-32pin (plastic)
  SRM20100LM70/85/10 SOP6-32pin (plastic)
  SRM20100LTM70/85/10 TSOP-32pin (plastic) *
  SRM20100LRM70/85/10 TSOPR-32pin (plastic)*

* : Under development

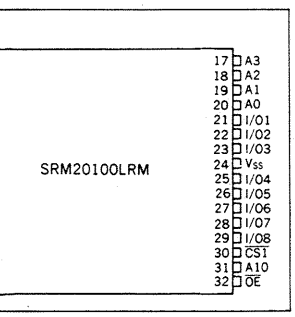
(DIP/SOP6)



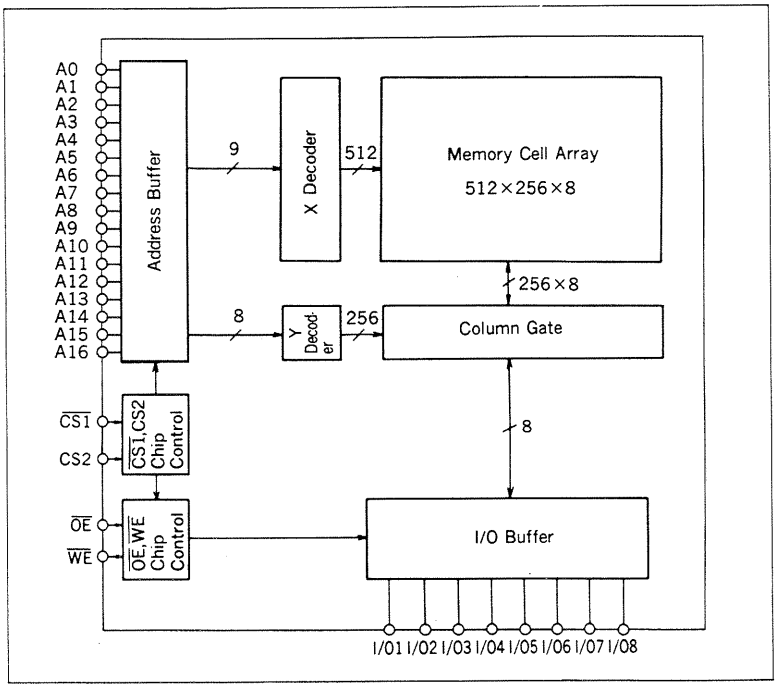
(TSOP)



(TSOPR)



■BLOCK DIAGRAM



■PIN DESCRIPTION

A0 to A16	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS1}$, CS2	Chip Select
I/O1 to 8	Data I/O
VDD	Power Supply(+5V)
Vss	Power Supply(0V)
NC	No connection

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage*	V_I	−0.5 to 7.0	V
Input/Output voltage*	$V_{I/O}$	−0.5 to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

* V_I, $V_{I/O}$ (Min)= −3.0V (Pulse width is 50ns)

■DC RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5.0	5.5	V
	V_{SS}	—	0	0	0	V
Input voltage	V_{IH}	—	2.2	3.5	V_{DD}+0.3	V
	V_{IL}	—	−0.3*	0	0.8	V

*If pulse width is less than 50ns, it is −3.0V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM20100LC$_{70}$			SRM20100LC$_{85}$			SRM20100LC$_{10}$			Unit
			Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	
Input leakage	I_{LI}	V_I=0 to V_{DD}	−1	—	1	−1	—	1	−1	—	1	μA
Standby supply current	I_{DDS}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	—	1.0	3.0	—	1.0	3.0	—	1.0	3.0	mA
	I_{DDS1}	$\overline{CS1}$=CS2≧V_{DD}−0.2V or CS2≦0.2V	—	2	100	—	2	100	—	2	100	μA
Average operating current	I_{DDA}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA t_{cyc}=Min	—	45	70	—	45	70	—	45	70	mA
Operating supply current	I_{DDO}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA	—	15	35	—	15	35	—	15	35	mA
Output leakage	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH} $V_{I/O}$=0 to V_{DD}	−1	—	1	−1	—	1	−1	—	1	μA
High level output voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	—	—	0.4	—	—	0.4	V

* Typcal values are measured at Ta=25°C and V_{DD}=5.0V

●Terminal Capacitance

(f=1MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C_{ADD}	V_{ADD}=0V	—	—	8	pF
Input Capacitance	C_I	V_I=0V	—	—	10	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	10	pF

●AC Electrical Characteristics

○Read Cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM20100LC$_{70}$		SRM20100LC$_{85}$		SRM20100LC$_{10}$		Unit
			Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	70	—	85	—	100	—	ns
Address access time	t_{ACC}		—	70	—	85	—	100	ns
Chip select 1 access time	t_{ACS1}		—	70	—	85	—	100	ns
Chip select 2 access time	t_{ACS2}		—	70	—	85	—	100	ns
Output enable access time	t_{OE}		—	40	—	45	—	50	ns
Chip select 1 output set time	t_{CLZ1}	*2	10	—	10	—	10	—	ns
Chip select 1 output floating	t_{CHZ1}		—	30	—	30	—	35	ns
Chip select 2 output set time	t_{CLZ2}		10	—	10	—	10	—	ns
Chip select 2 output floating	t_{CHZ2}		—	30	—	30	—	35	ns
Output enable output set time	t_{OLZ}		5	—	5	—	5	—	ns
Output enable output floating	t_{OHZ}		—	30	—	30	—	35	ns
Output hold time	t_{OH}	*1	10	—	10	—	10	—	ns

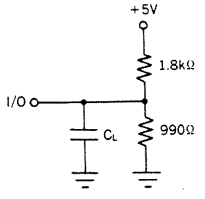
○ **Write Cycle**

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	SRM20100LC$_{70}$		SRM20100LC$_{85}$		SRM20100LC$_{10}$		Unit
			Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	70	—	85	—	100	—	ns
Chip select time 1	t_{CW1}		60	—	70	—	80	—	ns
Chip select time 2	t_{CW2}		60	—	70	—	80	—	ns
Address enable time	t_{AW}		60	—	70	—	80	—	ns
Address setup time	t_{AS}		0	—	0	—	0	—	ns
Write pulse width	t_{WP}		55	—	65	—	75	—	ns
Address hold time	t_{WR}		0	—	0	—	0	—	ns
Input data setup time	t_{DW}		30	—	35	—	40	—	ns
Input data hold time	t_{DH}		0	—	0	—	0	—	ns
$\overline{WE}$ Output floating	t_{WHZ}	*2	—	30	—	30	—	35	ns
$\overline{WE}$ Output setup time	t_{OW}		5	—	5	—	5	—	ns

*1 Test Conditions

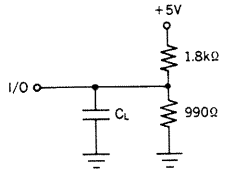
1. Input pulse level : 0.6V to 2.4V
2. tr = tf = 5ns
3. Input and output timing reference levels : 1.5V
4. Output load C_L = 100pF



C_L = 100pF (Includes Jig Capacitance)

*2 Test Conditions

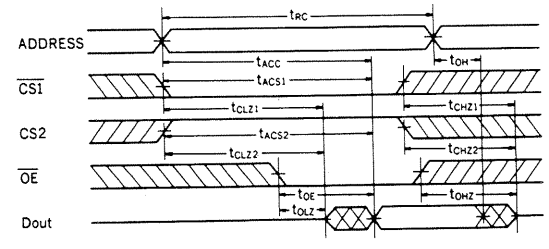
1. Input pulse level : 0.6V to 2.4V
2. tr = tf = 5ns
3. Input timing reference levels : 1.5V
4. Output timing reference levels : ±200mV (the level displaced from stable output voltage level)
5. Output load C_L = 5pF



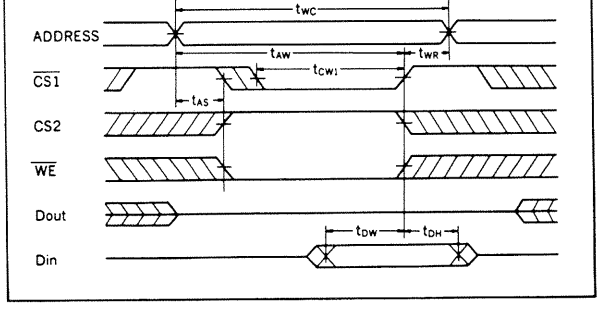
C_L = 5pF (Includes Jig Capacitance)

●Timing Chart

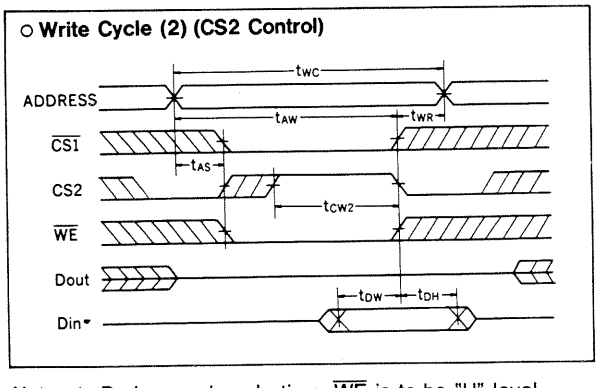
○ **Read Cycle**



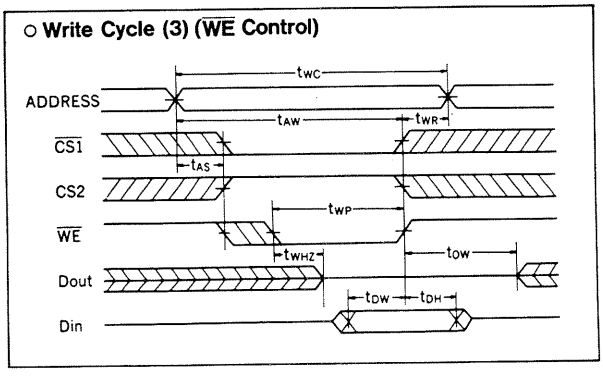
○ **Write Cycle (1) ($\overline{CS1}$ Control)**



○ **Write Cycle (2) (CS2 Control)**



○ **Write Cycle (3) ($\overline{WE}$ Control)**



Note : 1. During read cycle time, $\overline{WE}$ is to be "H" level.

2. During write cycle time that is controlled by $\overline{CS1}$ or CS2, Output Buffer is in high impedance state whether $\overline{OE}$ level is "H" or "L".
3. During write cycle time that is controlled by $\overline{WE}$, Output Buffer is high impedance state if $\overline{OE}$ is "H" level.
4. When I/O terminals are output mode, be careful that do not give the opposite signals to the I/O terminals.

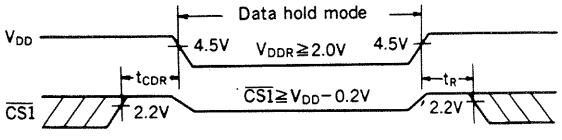
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(Ta = 0 to 70°C)

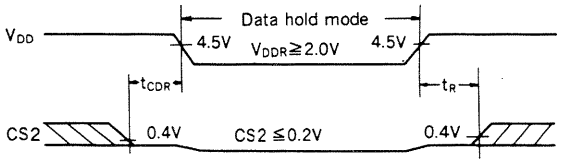
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	5.5	V
Data retention current	I_{DDR}	V_{DD} = 3V $\overline{CS1}$ = CS2 ≧ V_{DD} − 0.2V or CS2 ≦ 0.2V	—	1 *1	50	μA
Chip select·data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		t_{RC} *2	—	—	ns

*1 Ta = 25°C
*2 t_{RC} = Read cycle time

Data retention timing ($\overline{CS1}$ Control)



Data retention timing (CS2 Control)



■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	DATA I/O	Mode	I_{DD}
H	X	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
—	L	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
L	H	X	L	Input data	Write	I_{DDO}
L	H	L	H	Output data	Read	I_{DDO}
L	H	H	H	Hi-Z	Output disable	I_{DDO}

X : "H" or "L", — : "H", "L" or "Hi-Z"

● Reading data

Data is able to be read when the address is setted while holding $\overline{CS1}$ = "L", CS2 = "H", $\overline{OE}$ = "L" and $\overline{WE}$ = "H". Since Data I/O terminals are in high impedance state when $\overline{OE}$ = "H", the data bus line can be used for any other objective, then access time apparently is able to be cut down.

● Writing data

There are the following four ways of writing data into the memory.

(1) Hold CS2 = "H", $\overline{WE}$ = "L" set addresses and give "L" pulse to $\overline{CS1}$.
(2) Hold $\overline{CS1}$ = "L", $\overline{WE}$ = "L", set addresses and give "H" pulse to CS2.
(3) Hold $\overline{CS1}$ = "L", CS2 = "H", set addresses and give "L" pulse to $\overline{WE}$.
(4) After setting addresses, give "L" pulse to $\overline{CS1}$, $\overline{WE}$ and give "H" pulse to CS2.

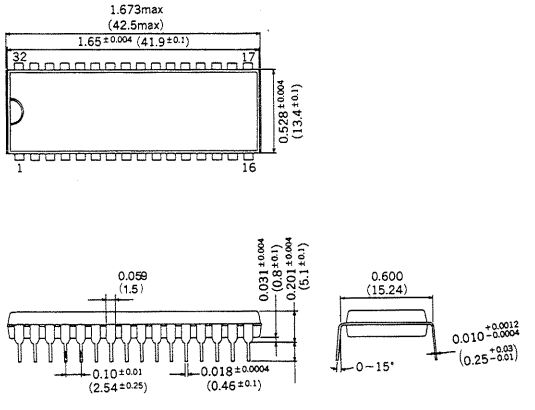
Anyway, data on the Data I/O terminals are latched up into the SRM20100LC$_{70/85/10}$ at the end of the period that $\overline{CS1}$, $\overline{WE}$ are "L" level, and CS2 is "H" level. As Data I/O terminals are in high impedance state when any of $\overline{CS1}$, $\overline{OE}$ = "H", or CS2 = "L", the contention on the data bus can be avoided.

● **Standby mode**

When $\overline{CS1}$ is "H" or CS2 is "L" level, the SRM20100LC$_{70/85/10}$ is in the standby mode which has retaning date operation. In this case Data I/O terminals are Hi-Z, and all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L". When $\overline{CS1}$ and CS2 level are in the range over V_{DD}-0.2V, or CS2 level is in the range under 0.2V, in the SRM20100LC$_{70/85/10}$ there is almost no current flow except through the high resistance parts of the memory.

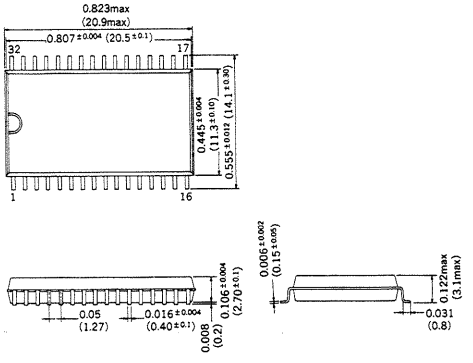
■PACKAGE DIMENSIONS

Plastic DIP-32pin



unit : inch
(mm)

Plastic SOP6-32pin*1

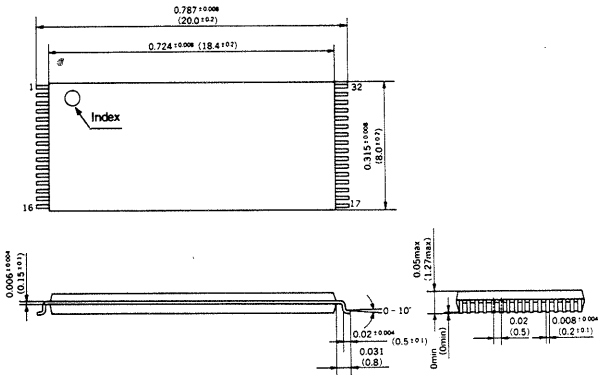


unit : inch
(mm)

*1 SRM20100LM$_{70/85/10}$ has the same characteristics as SRM20100LC$_{70/85/10}$.

Plastic TSOP-32pin*1

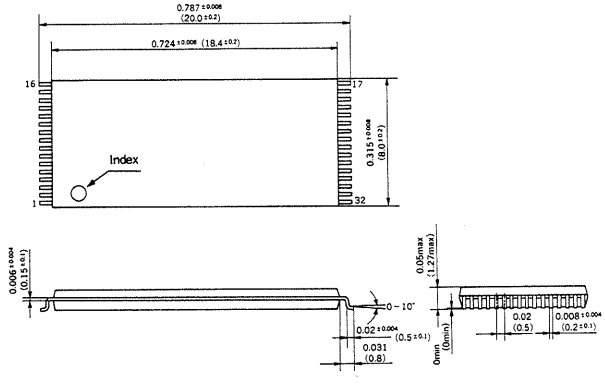
(Under development)



*1 SRM20100LTM70/85/100 has the same characteristics as SRM20100LC70/85/10.

Plastic TSOPR-32pin*2

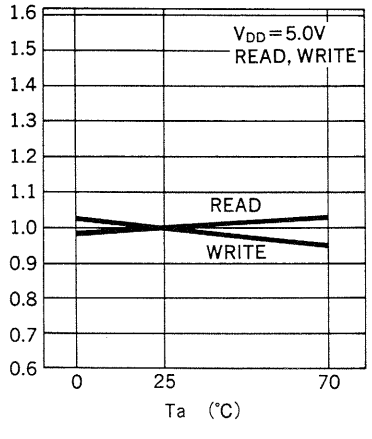
(Under development)



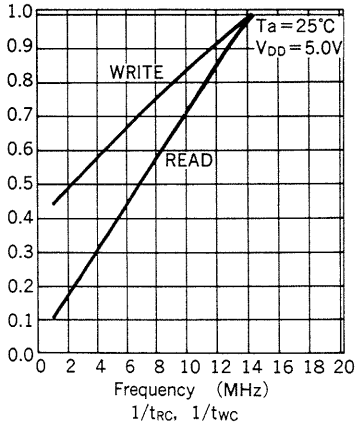
*2 SRM20100LRM70/85/100 has the same characteristics as SRM20100LC70/85/10.

■CHARACTERISTICS CURVES

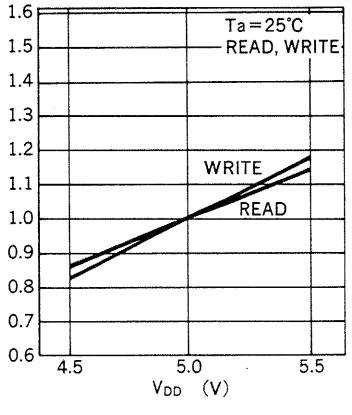
Normalized I_{DDA}—Ta



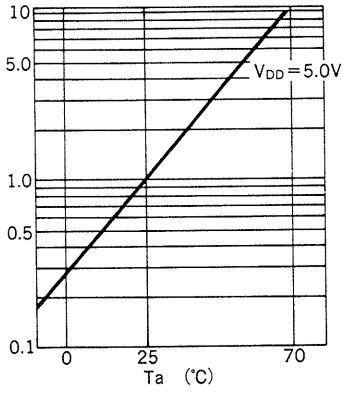
Normalized I_{DDA}—Frequency



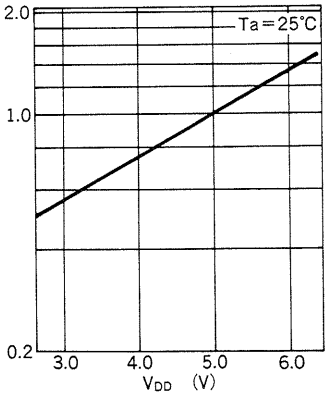
Normalized I_{DDA}—V_{DD}



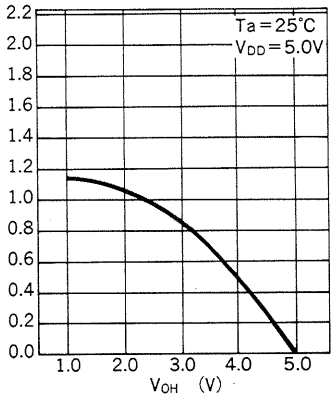
Normalized I_{DDS1}—Ta



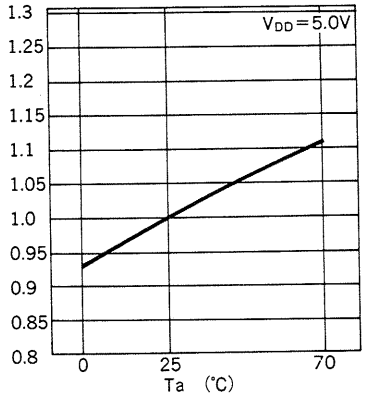
Normalized I_{DDS1}—V_{DD}



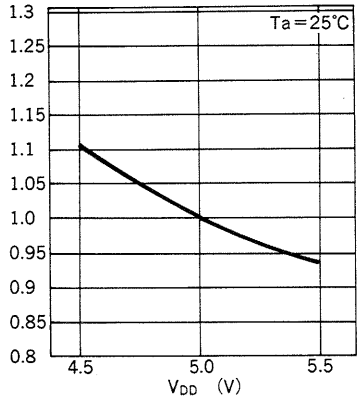
Normalized I_{OH}—V_{OH}



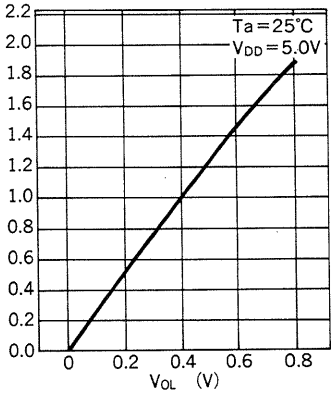
t_{ACC}
Normalized t_{ACS1}
t_{ACS2}—Ta



t_{ACC}
Normalized t_{ACS1}
t_{ACS2}—V_{DD}



Normalized I_{OL}—V_{OL}



t_{ACC}
Normalized t_{ACS1}
t_{ACS2}—C_L