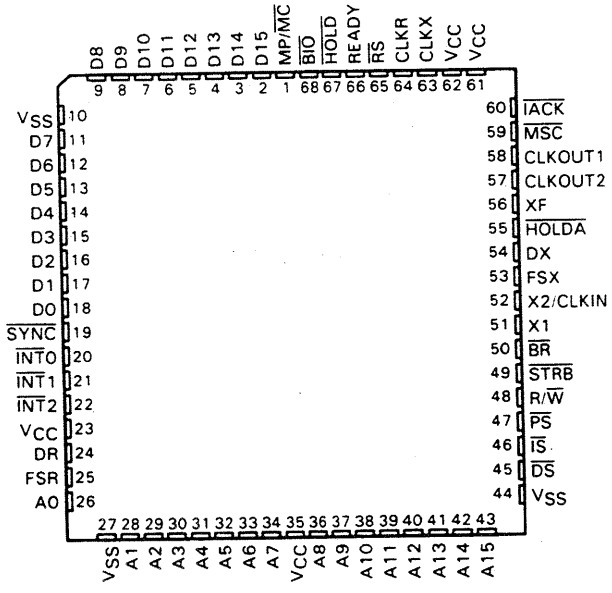
TMS320C26FNL
DIGITAL SIGNAL PROCESSOR

JANUARY 1989

- 100-ns Instruction Cycle Time
- 1568 Words of Programmable On-Chip Data RAM
- TMS320C25 pin for pin compatible
- TMS320C25 object code compatible except for RAM configuration instructions
- 256 Words of On-Chip Program ROM
- 128k Words of Data/Program Space
- Sixteen Input and Sixteen Output Channels
- 16-Bit Parallel Interface
- Directly Accessible External Data Memory Space
- Global Data Memory Interface
- 16-Bit Instruction and Data Words
- 32-Bit ALU and Accumulator
- Single-Cycle Multiply/Accumulate Instructions
- 0 to 16-Bit Scaling Shifter
- Bit Manipulation and Logical Instructions
- Instruction Set Support for Floating-Point Operations. Adaptive Filtering, and Extended-Precision Arithmetic
- Block Moves for Data/Program Management
- Repeat Instructions for Efficient Use of Program Space
- Eight Auxiliary Registers and Dedicated Arithmetic Unit for Indirect Addressing
- Serial Port for Direct Codec Interface
- Synchronization Input for Synchronous Multiprocessor Configurations
- Wait States for Communication to Slow Off-Chip Memories/Peripherals
- On-Chip Timer for Control Operations
- Three External Maskable User Interrupts
- Input Pin Polled by Software Branch Instruction
- Programmable Output Pin for Signalling External Devices
- 1.8-μm CMOS Technology
- Single 5-V Supply
- On-Chip Clock Generator

68-PIN FN
PLASTIC LEADED CHIP CARRIER PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS

PIN NOMENCLATURE

SIGNALS	I / O / Z*	DEFINITION
V_{CC}	I	5 - V supply pins.
V_{SS}	I	Ground pins.
X1	O	Output from internal oscillator for crystal.
X2 / CLKIN	I	Input to internal oscillator from crystal or external clock.
CLKOUT1	O	Master clock output (crystal or CLKIN frequence / 4).
CLKOUT2	O	A second clock output signal.
D15 - D0	I / O / Z	16 - bit data bus D15 (MSB) through DO (LSB). Multiplexed between program, data and I / O spaces.
A15 - A0	O / Z	16 - bit address bus A15 (MSB) through AO (LSB).
$\overline{PS}.\overline{DS}.\overline{IS}$	O / Z	Program, data and I / O space select signals.
R / $\overline{W}$	O / Z	Read / write signal.
$\overline{STRB}$	O / Z	Strobe signal.
$\overline{RS}$	I	Reset input.
$\overline{INT2}.\overline{INT0}$	I	External user interrupt inputs.
MP/$\overline{MC}$	I	Microprocessor microcomputer mode select pin.
$\overline{MSC}$	O	Microstate complete signal.
$\overline{IACK}$	O	Interrupt acknowledge signal.
READY	I	Data ready inptu. Asserted by external logic when using slower devices to indicate that the current bus transaction is complete.
$\overline{BR}$	O	Bus request signal. Asserted when the TMX320C26 requires access to an external global data memory space.
XF	O	External flag output (latched software - programmable signal).
$\overline{HOLD}$	I	Hold input. When asserted. TMX320C26 goes into an idle mode and places the data address and control lines in the high - impedance state.
$\overline{HOLDA}$	O	Hold acknowledge signal.
$\overline{SYNC}$	I	Synchronization input.
$\overline{BIO}$	I	Branch control input. Polled by BIOZ instrution.
DR	I	Serial data receive inptu.
CLKR	I	Clock for receive inptut for serial port.
FSR	I	Frame synchronization pulse for receive inptut.
DX	O / Z	Serial data transmit ouput.
CLKX	I	Clock for transmit output for serial port.
FSX	I / O / Z	Frame synchronization pulse for transmit. Configuration as either an input or an output.

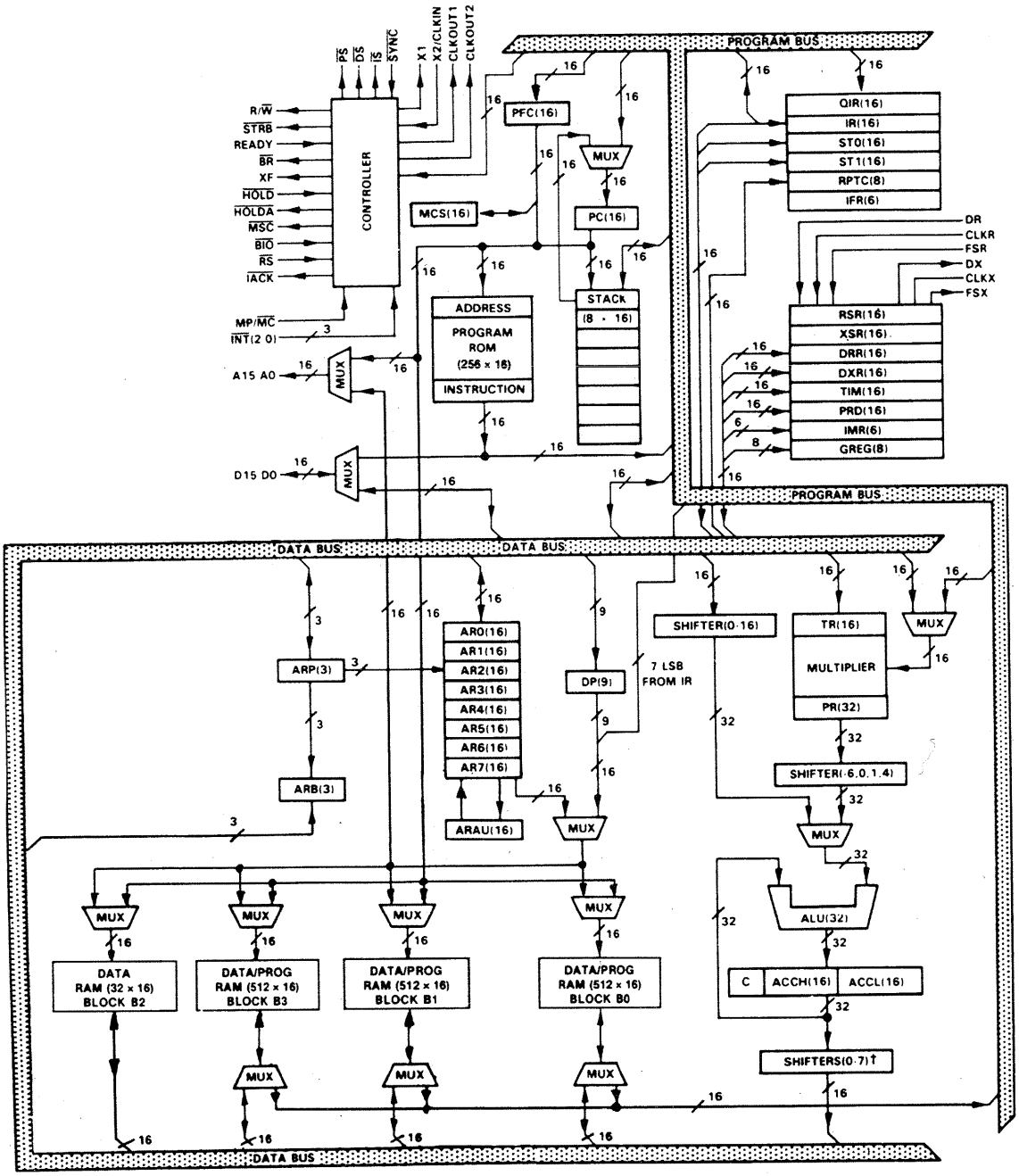
*I / O / Z denotes input / output / high - impedance state.

description

The TMS320C26 Digital Signal Processor is a member of the TMS320 family of VLSI digital signal processors and peripherals. The TMS320 family supports a wide range of digital signal processing applications, such as telecommunications, modems, image processing, speech processing, spectrum analysis, audio processing, digital filtering, high-speed control, graphics, and other computation intensive applications.

With a 100-ns instruction cycle time and an innovative memory configuration, the TMS320C26 performs operations necessary for many real time digital signal processing algorithms. Since most instructions require only one cycle, the TMS320C26 is capable of executing ten million instructions per second. On-chip data RAM of 1568 words of 16 bits, on-chip program ROM of 256-words, direct addressing of up to 64K-words of external data memory space and 64K-words of external program memory space, and multiprocessor interface features for sharing global memory minimize unnecessary data transfers to take full advantage of the capabilities of the processor.

functional block diagram (TMS320C26)



LEGEND:

ACCH	= Accumulator high	IFR	= Interrupt flag register	PC	= Program counter
ACCL	= Accumulator low	IMR	= Interrupt mask register	PFC	= Prefetch counter
ALU	= Arithmetic logic unit	IR	= Instruction register	RPTC	= Repeat instruction counter
ARAU	= Auxiliary register arithmetic unit	MCS	= Microcall stack	GREG	= Global memory allocation register
ARB	= Auxiliary register pointer buffer	QIR	= Queue instruction register	RSR	= Serial port receive shift register
ARP	= Auxiliary register pointer	PR	= Product register	XSR	= Serial port transmit shift register
DP	= Data memory page pointer	PRD	= Period register for timer	AR0-AR7	= Auxiliary registers
DRR	= Serial port data receive register	TIM	= Timer	ST0,ST1	= Status registers
DXR	= Serial port data transmit register	TR	= Temporary register	C	= Carry bit

architecture

The TMS320C26 architecture is based on the TMS320C25 with a different internal RAM and ROM configuration. The TMS320C26 integrates 256 words of on-chip ROM and 1568 words of on-chip RAM compared to 4K words of on-chip ROM and 544 words of on-chip RAM for the TMS320C25. The TMS320C26 is pin for pin compatible with the TMS320C25.

Increased throughput on the TMS320C26 for many DSP applications is accomplished by means of single-cycle multiply/accumulate instructions with a data move option, eight auxiliary registers with a dedicated arithmetic unit, and faster I/O necessary for data intensive signal processing.

The architectural design of the TMS320C26 emphasizes overall speed, communication, and flexibility in processor configuration. Control signals and instructions provide floating point support, block memory transfers, communication to slower off-chip devices, and multiprocessing implementations.

Three large on-chip RAM blocks, configurable either as separate program and data spaces or as three contiguous data blocks, provide increased flexibility in system design. Programs of up to 256 words can be masked into the internal program ROM. The remainder of the 64K-word program memory space is located externally. Large programs can execute at full speed from this memory space. Programs can also be downloaded from slow external memory to high speed on-chip RAM. A total of 64K data memory address space is included to facilitate implementation of DSP algoritms. The VLSI implementation of the TMS20C26 incorporates all of these features as well as many others, such as a hardware timer, serial port, and block data transfer capabilities.

32-bit ALU/accumulator

The TMS320C26 32-bit Arithmetic Logic Unit (ALU) and accumulator perform a wide range of arithmetic and logic instructions, the majority of which execute in a single clock cycle. The ALU executes a variety of branch instructions dependent on the status of the ALU or a single bit in a word. These instructions provide the following capabilities:

- Branch to an address specified by the accumulator.
- Normalize fixed point numbers contained in the accumulator.
- Test a specified bit of a word in data memory.

One input to the ALU is always provided from the accumulator, and the other input may be provided from the Product Register (PR) of the multiplier or the input scaling shifter which has fetched data from the RAM on the data bus. After the ALU has performed the arithmetic or logical operations, the result is stored in the accumulator.

The 32-bit accumulator is split into two 16-bit segments for storage in data memory. Additional shifters at the output of the accumulator perform shifts while the data is being transferred to the data bus for storage. The contents of the accumulator remain unchanged.

scaling shifter

The TMS320C26 scaling shifter has a 16-bit input connected to the data bus and a 32-bit output connected to the ALU. The scaling shifter produces a left shift of 0 to 16-bits on the input data, as programmed in the instruction. The LSBs of the output are filled with zeroes, and the MSBs may be either filled with zeroes or sign extended, depending upon the status programmed into the SXM (sign extension mode) bit of status register STO.

16 × 16 bit parallel multiplier

The TMS320C26 has a 16 × 16 bit-hardware multiplier, which is capable of computing a signed or unsigned 32-bit product in a single machine cycle. The multiplier has the following two associated registers:

- A 16-bit Temporary Registers (TR) that holds one of the operands for the multiplier, and
- A 32-bit Product Register (PR) that holds the product.

Incorporated into the TMS320C26 instruction set are single-cycle multiply/accumulate instructions that allow both operands to be processed simultaneously. The data for these operations may reside anywhere in internal or external memory, and can be transferred to the multiplier each cycle via the program and data buses.

Four product shift modes are available at the Product Register (PR) output that are useful when performing multiply/accumulate operations, fractional arithmetic, or justifying fractional products.

timer

The TMS320C26 provides a memory mapped 16-bit timer for control operations. The on-chip timer (TIM) register is a down counter that is continuously clocked by CLKOUT 1. A timer interrupt (TINT) is generated every time the timer decrements to zero. The timer is reloaded with the value contained in the period (PRD) register within the next cycle after it reaches zero so that interrupts may be programmed to occur at regular intervals of PRD + 1 cycles of CLKOUT 1.

memory control

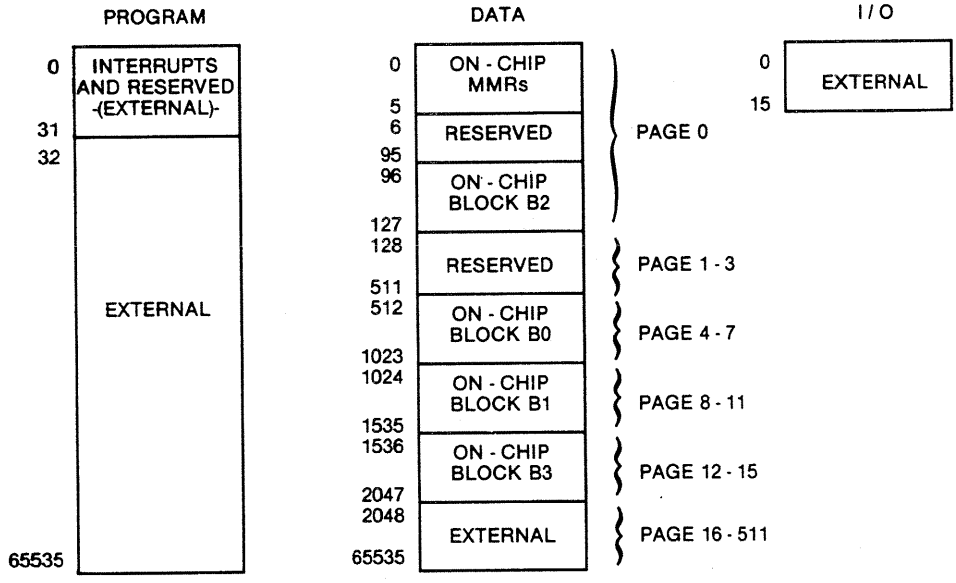
The TMS320C26 provides a total of 1568 words of 16 bit on-chip data RAM, divided into four separate blocks (B0, B1, B2, and B3). Of the 1568 words, 32 words (block B2) are always data memory, and all other words are programmable as either data or program memory. A data memory size of 1568 words allows the TMS320C26 to handle a data array of 1536 words, while still leaving 32 locations for intermediate storage. When using B0, B1, or B3 as program memory, instructions can be downloaded from external program memory into on-chip RAM, and then executed.

When using on-chip program RAM, ROM, or high speed external program memory, the TMS320C26 runs at full speed without wait states. However, the READY line can be used to interface the TMS320C26 to slower, less expensive external memory. Downloading programs from slow off-chip memory to on-chip program RAM speeds processing and cuts system costs.

The TMS320C26 provides three separate address spaces for program memory, data memory, and I/O. The on-chip memory is mapped into either the 64K-word data memory or program memory space, depending upon the choice of memory configuration. The CONF 0 (configure all blocks as data memory), CONF 1 (configure block B0 as program memory), CONF 2 (configure block B0 and B1 as program memory) and CONF 3 (configure B0, B1, and B3 as program memory) instructions allow dynamic configuration of the memory maps through software. Regardless of the configuration, the user may still execute from external program memory.

The TMS320C26 has six registers that are mapped into the data memory space at the first addresses; a serial port data receive register, serial port data transmit register, timer register, period register, interrupt mask register, and global memory allocation register.

A. MEMORY MAPS AFTER A RESET OR CONF 0
A. 1 MP/MC = 1



A.2 MP/MC = 0

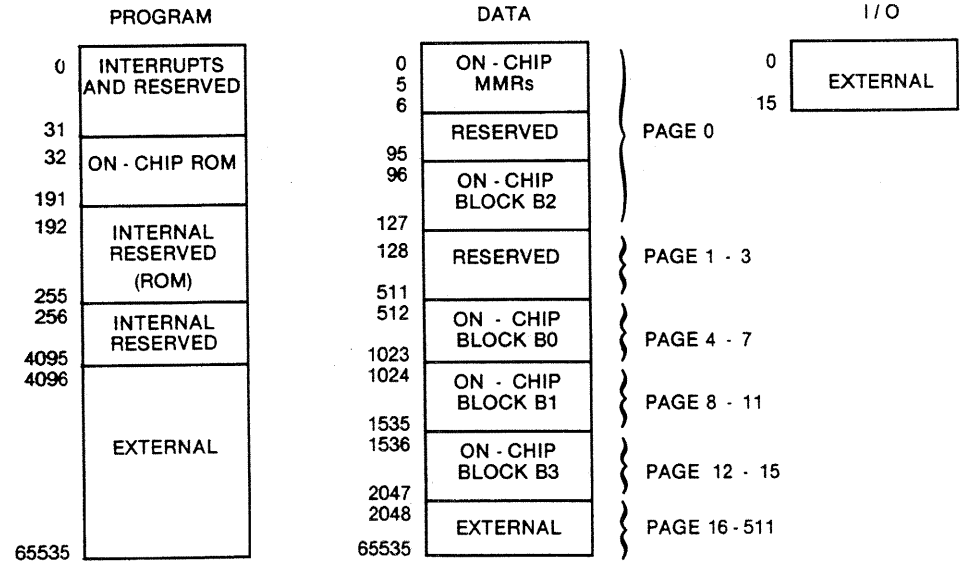
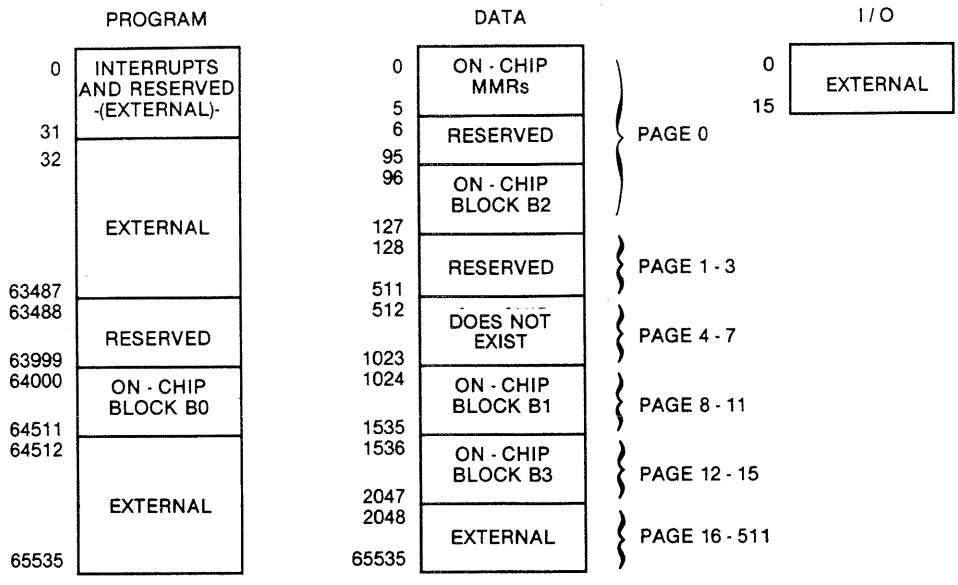


Figure 1a. Memory maps

B. MEMORY MAPS AFTER CONF 1
B. 1 MP/MC = 1



B.2 MP / MC = 0

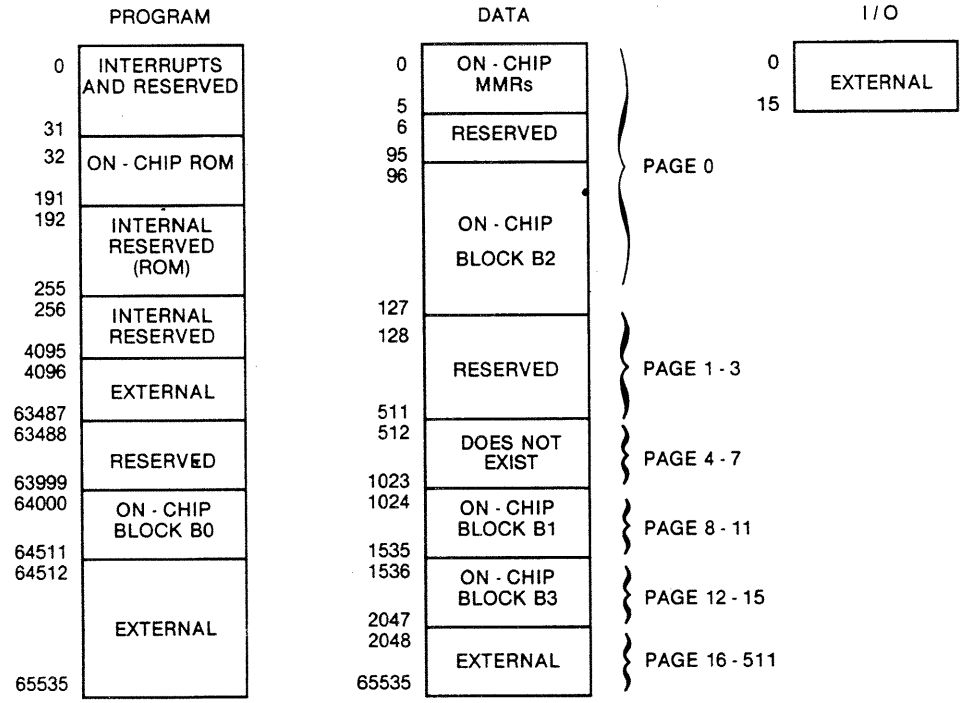
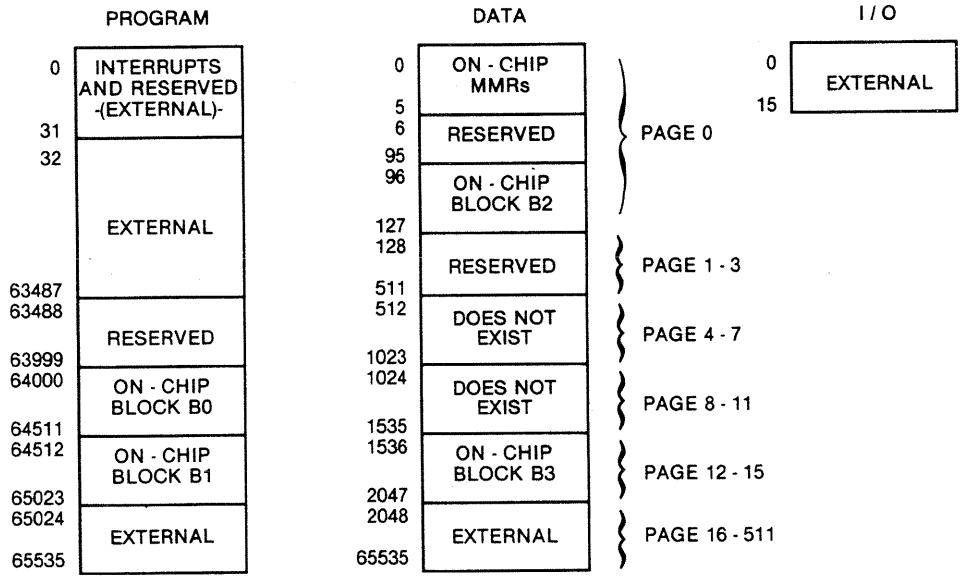


Figure 1b. Memory maps

C. MEMORY MAPS AFTER CONF 2
C. 1 MP/MC = 1



C.2 MP/MC = 0

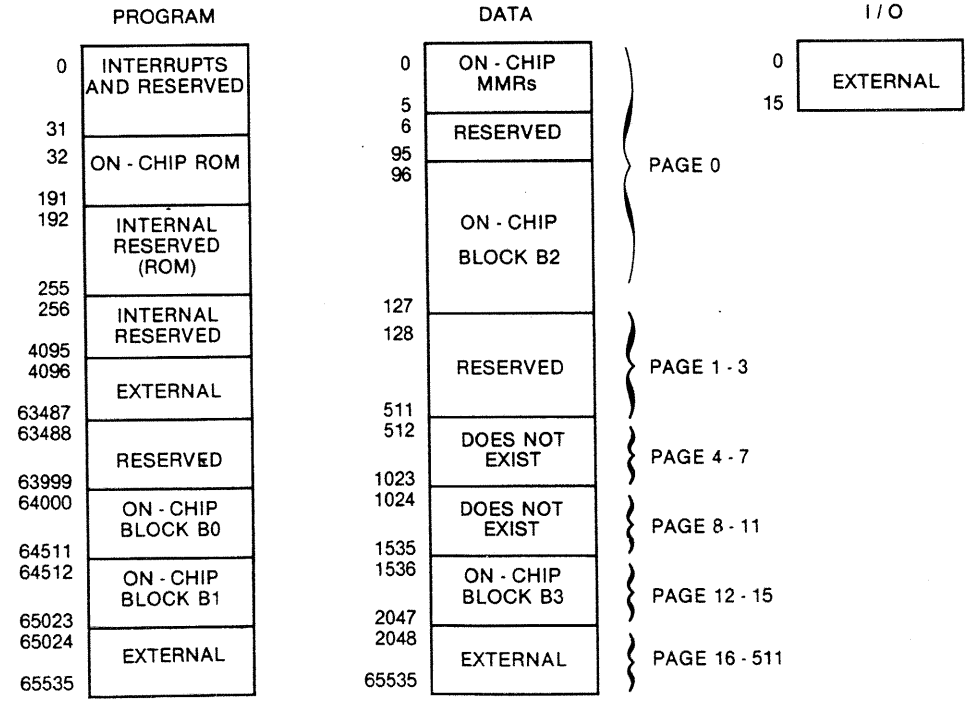


Figure 1c. Memory maps

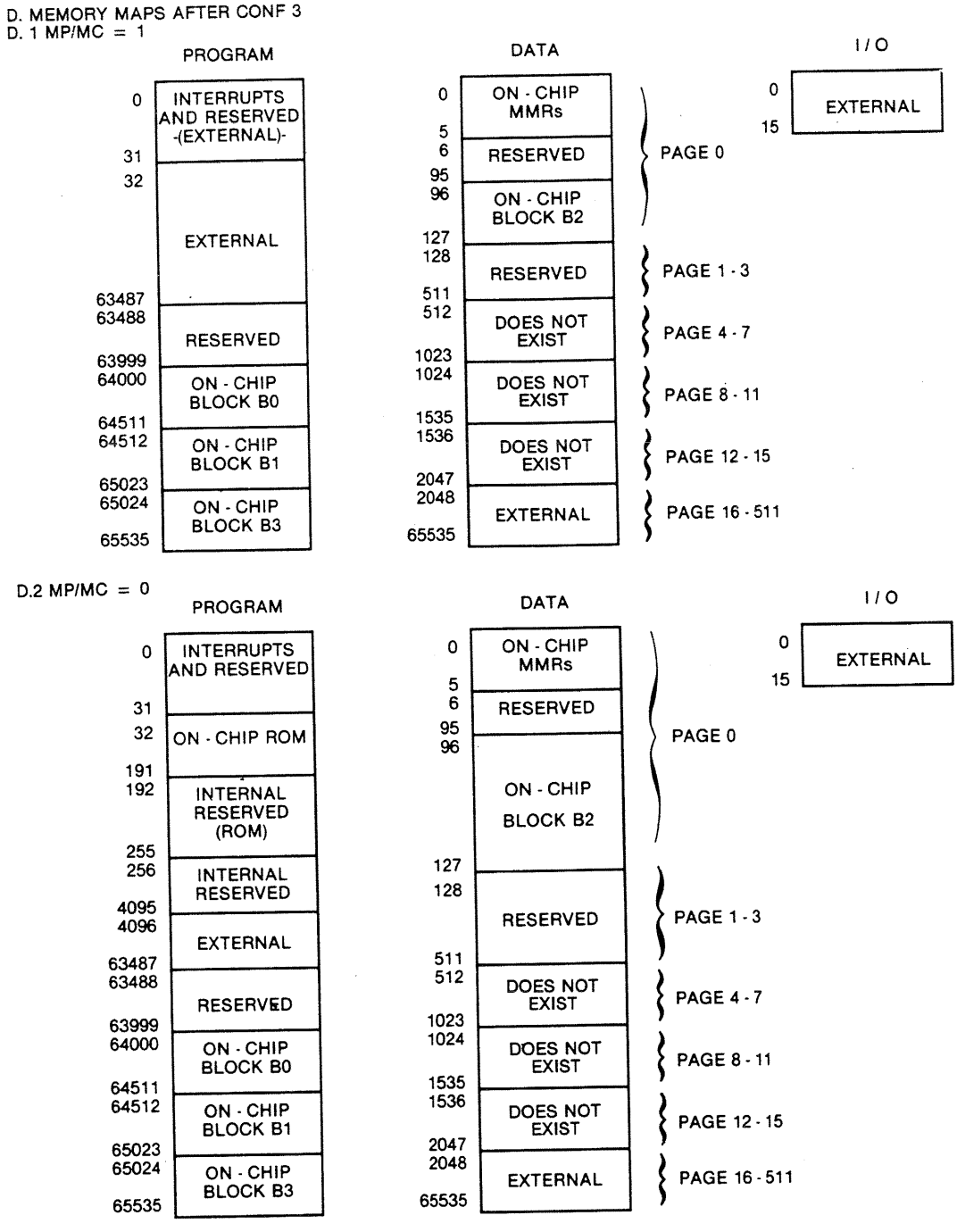


Figure 1d. Memory maps

interrupts and subroutine

The TMS320C26 has three external maskable user interrupts $\overline{\text{INT}}$ 2 — $\overline{\text{INT}}$ 0, available for external devices that interrupt the processor. Internal interrupts are generated by the serial port (RINT and XINT), by the timer (TINT), and by the software interrupt (TRAP) instruction. Interrupts are prioritized with reset ($\overline{\text{RS}}$) having the highest priority and the serial port transmit interrupt (XINT) having the lowest priority. All interrupt locations are on two-words boundaries so that branch instructions can be accommodated in those locations if desired.

A built in mechanism protects multicycle instructions from interrupts. If an interrupt occurs during a multicycle instruction, the interrupt is not processed until the instruction is completed. This mechanism applies both to instructions that are repeated or become multicycle due to the READY signal.

external interface

The TMS320C26 supports a wide range of system interfacing requirements. Program, data, and I/O address spaces provide interface to memory and I/O, this maximizing system throughput. I/O design is simplified by having I/O treated the same way as memory. I/O devices are mapped into the I/O address space using the processor's external address and data busses in the same manner as memory-mapped devices. Interface to memory and I/O devices of varying speeds is accomplished by using the READY line. When transactions are made with slower devices, the TMS320C26 processor waits untill the other device completes its function and signals the processor via the READY line. Then, the TMS320C26 continues execution.

A serial port provides communication with serial devices, such as codecs, serial A/D converters, and other serial systems. The interface signals are compatible with codecs and many other serial devices with a minimum of external hardware. The serial port may also be used for intercommunication between processors in multiprocessing applications.

The serial port has two memory mapped registers; the data transmit register (DXR) and the data receive register (DRR). Both registers operate in either the byte mode or 16-bit word mode, and may be accessed in the same manner as any other data memory location. Each register has an external clock, a framing synchronization pulse, and associated shift registers. One method of multiprocessing may be implemented by programming one device to transmit while the others are in the receive mode.

multiprocessing

The flexibility of the TMS320C26 allows configurations to satisfy a wide range of system requirements. The TMS320C26 can be used as follows:

- A standalone processor.
- A multiprocessor with devices in parallel
- A multiprocessor with global memory space.
- A peripheral processor interfaced via processor controlled signals to another device.

For multiprocessing applications, the TMS320C26 has the capability of allocating global data memory space and communicating with that space via the $\overline{BR}$ (bus request) and READY control signals. Global memory is data memory shared by more than one processor. Global data memory access must be arbitrated. The 8-bit memory mapped GREG (global memory allocation register) specifies part of the TMS320C26's data memory as global external memory. The contents of the register determine the size of the global memory space. If the current instruction addresses and operand within that space, $\overline{BR}$ is asserted to request control of the bus. The length of the memory cycle is controlled by the READY line.
The TMS320C26 supports DMA (direct memory access) to its external program/data memory using the $\overline{HOLD}$ and $\overline{HOLDA}$ signals. Another processor can take complete control of the TMS320C26's external memory by asserting $\overline{HOLD}$ low. This causes the TMS320C26 to place its address, data, and control lines in a high impedance state, and assert $\overline{HOLDA}$.

instruction set

The TMS320C26 microprocessor implements a comprehensive instruction set that supports both numeric intensive signal processing operations as well as general purpose applications, such as multiprocessing and high speed control.

For maximum throughput, the next instruction is prefetched while the current one is being executed. Since the same data lines are used to communicate to external data/program or I/O space, the number of cycles may vary depending upon whether the next data operand fetch is from internal or external program memory. Highest throughput is achieved by maintaining data memory on-chip and using either internal or fast external program memory.

addressing modes

The TMS320C26 instruction set provides three memory addressing modes: direct, indirect, and immediate addressing.

Both direct and indirect addressing can be used to access data memory. In direct addressing, seven bits of the instruction word are concatenated with the nine bits of the data memory page pointer to form the 16-bit data memory address. Indirect addressing accesses data memory through the eight auxiliary registers. In immediate addressing, the data is based on a portion of the instruction word (s).

In direct memory addressing, the instruction word contains the lower seven bits of the data memory address. This field is concatenated with the nine bits of the data memory page pointer to form the full 16-bit address. Thus, memory is paged in the direct addressing mode with a total of 512 pages, each page containing 128 words.

Eight auxiliary registers (AR0-AR7) provide flexible and powerful indirect addressing. To select a specific auxiliary register, the Auxiliary Register Pointer (ARP) is loaded with a value from 0 through 7 for AR0 through AR7 respectively.

There are seven types of indirect addressing: auto increment, auto decrement, post indexing by either adding or subtracting the contents of AR0, single indirect addressing with no increment or increment and bit reversal addressing (used in FFTS) with increment or decrement. All operations are performed on the current auxiliary register in the same cycle as the original instruction, followed by a new ARP value being loaded.

repeat feature

A repeat feature, used with instructions such as multiply/accumulates, block moves, I/O transfers, and table read/writes, allows a single instruction to be performed up to 256 times. The repeat counter (RPTC) is loaded with either a data memory value (RPT instruction) or an immediate value (RPTK instruction). The value of this operand is one less than the number of times that the next instruction is executed. Those instructions that are normaly multicycle are pipelined when using the repeat feature, and effectively become cycle instructions.

instruction set summary

Table 1 lists the symbols and abbreviations used in Table 2, the instruction set summary. Table 2 consists primarily of single-cycle, single-word instructions. Infrequently used branch, I-O, and CALL instructions are multicycle. The instruction set summary is arranged according to function and alphabetized within each functional grouping. The symbol (+) indicates those instructions that are not included in the TMS32010 instruction set. The symbol (±) indicates instructions that are not included in the TMS32020 instruction set. The symbol (#) indicates instructions that are not included in the TMS320C25 instruction set.

TABLE 1. INSTRUCTION SYMBOLS

SYMBOL	MEANING
B	4 - bit field specifying a bit code
CM	2 - bit field specifying compare mode
D	Data memory address field
FO	Format status bit
I	Addressing mode bit
K	Immediate operand field
PA	Port address (PAO through PA 15 are predefined assembler symbols equal to 0 through 15 respectively.)
PM	2 - bit field specifying P register output shift code
R	3 - bit operand field specifying auxiliary register
S	4 - bit left-shift code
X	3 - bit accumulator left-shift field

TABLE 2. TMS320C26 INSTRUCTION SET SUMMARY

ACCUMULATOR MEMORY REFERENCE INSTRUCTIONS			
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE
			15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ABS	Absolute value of accumulator	1	1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 1
ADD	Add to accumulator with shift	1	0 0 0 0 ←S→ I ←D→
ADDC‡	Add to accumulator with carry	1	0 1 0 0 0 0 1 1 I ←D→
ADDH	Add to high accumulator	1	0 1 0 0 1 0 0 0 I ←D→
ADDK‡	Add to accumulator short immediate	1	1 1 0 0 1 1 0 0 ←K→
ADDS	Add to low accumulator with sign extension suppressed	1	0 1 0 0 1 0 0 1 I ←D→
ADDT†	Add to accumulator with shift specified by T register	1	0 1 0 0 1 0 1 0 I ←D→
ADLK†	Add to accumulator long immediate with shift	2	1 1 0 1 ←S→ 0 0 0 0 0 0 1 0
AND	AND with accumulator	1	0 1 0 0 1 1 1 0 I ←D→
ANDK†	AND immediate with accumulator with shift	2	1 1 0 1 ←S→ 0 0 0 0 0 1 0 0
CMPL†	Complement accumulator	1	1 1 0 0 1 1 1 0 0 0 1 0 0 1 1 1
LAC	Load accumulator with shift	1	0 0 1 0 ←S→ I ←D→
LACK	Load accumulator immediate short	1	1 1 0 0 1 0 1 0 ←K→
LACT†	Load accumulator with shift specified by T register	1	0 1 0 0 0 0 1 0 I ←D→
LALK†	Load accumulator long immediate with shift	2	1 1 0 1 ←S→ 0 0 0 0 0 0 0 1
NEG†	Negate accumulator	1	1 1 0 0 1 1 1 0 0 0 1 0 0 0 1 1
NORM†	Normalize contents of accumulator	1	1 1 0 0 1 1 1 0 1 ←D→
OR	OR with accumulator	1	0 1 0 0 1 1 0 1 I ←D→
ORK†	OR immediate with accumulator with shift	2	1 1 0 1 ←S→ 0 0 0 0 0 1 0 1
ROL‡	Rotate accumulator left	1	1 1 0 0 1 1 1 0 0 0 1 1 0 1 0 0
ROR‡	Rotate accumulator right	1	1 1 0 0 1 1 1 0 0 0 1 1 0 1 0 1
SACH	Store high accumulator with shift	1	0 1 1 0 1 ←X→ I ←D→
SACL	Store low accumulator with shift	1	0 1 1 0 0 ←X→ I ←D→
SBLK†	Subtract from accumulator long immediate with shift	2	1 1 0 1 ←S→ 0 0 0 0 0 0 1 1
SFL†	Shift accumulator left	1	1 1 0 0 1 1 1 0 0 0 0 1 1 0 0 0
SFR†	Shift accumulator right	1	1 1 0 0 1 1 1 0 0 0 0 1 1 0 0 1
SUB	Subtract from accumulator with shift	1	0 0 0 1 ←S→ I ←D→
SUBB‡	Subtract from accumulator with borrow	1	0 1 0 0 1 1 1 1 I ←D→
SUBC	Conditional subtract	1	0 1 0 0 0 1 1 1 I ←D→
SUBH	Subtract from high accumulator	1	0 1 0 0 0 1 0 0 I ←D→
SUBK‡	Subtract from accumulator short immediate	1	1 1 0 0 1 1 0 1 ←K→
SUBS	Subtract from low accumulator with sign extension suppressed	1	0 1 0 0 0 1 0 1 I ←D→
SUBT†	Subtract from accumulator with shift specified by T register	1	0 1 0 0 0 1 1 0 I ←D→
XOR	Exclusive-OR with accumulator	1	0 1 0 0 1 1 0 0 I ←D→
XORK†	Exclusive-OR immediate with accumulator with shift	2	1 1 0 1 ←S→ 0 0 0 0 0 1 1 0
ZAC	Zero accumulator	1	1 1 0 0 1 0 1 0 0 0 0 0 0 0 0 0
ZALH	Zero low accumulator and load high accumulator	1	0 1 0 0 0 0 0 0 I ←D→
ZALR‡	Zero low accumulator and load high accumulator with rounding	1	0 1 1 1 1 0 1 1 I ←D→
ZALS	Zero accumulator and load low accumulator with sign extension suppressed	1	0 1 0 0 0 0 0 1 I ←D→

†These instructions are not included in the TMS32010 instruction set.
‡These instructions are not included in the TMS32020 instruction set.

TABLE 2. TMS320C26 INSTRUCTION SET SUMMARY (CONTINUED)

AUXILIARY REGISTERS AND DATA PAGE POINTER INSTRUCTIONS			
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE
ADRK‡	Add to auxiliary register short immediate	1	0 1 1 1 1 1 1 0 ◄——K——►
CMPR†	Compare auxiliary register with auxiliary register AR0	1	1 1 0 0 1 1 1 0 0 1 0 1 0 0 ◄CM►
LAR	Load auxiliary register	1	0 0 1 1 0 ◄—R—► I ◄——D——►
LARK	Load auxiliary register short immediate	1	1 1 0 0 0 ◄—R—► ◄——K——►
LARP	Load auxiliary register pointer	1	0 1 0 1 0 1 0 1 1 0 0 0 1 ◄—R—►
LDP	Load data memory page pointer	1	0 1 0 1 0 0 1 0 I ◄——D——►
LDPK	Load data memory page pointer immediate	1	1 1 0 0 1 0 0 ◄——DP——►
LRLK†	Load auxiliary register long immediate	2	1 1 0 1 0 ◄—R—► 0 0 0 0 0 0 0 0
MAR	Modify auxiliary register	1	0 1 0 1 0 1 0 1 I ◄——D——►
SAR	Store auxiliary register	1	0 1 1 1 0 ◄—R—► I ◄——D——►
SBRK‡	Subtract from auxiliary register short immediate	1	0 1 1 1 1 1 1 1 ◄——K——►

T REGISTER, P REGISTER, AND MULTIPLY INSTRUCTIONS			
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE
APAC	Add P register to accumulator	1	1 1 0 0 1 1 1 0 0 0 0 1 0 1 0 1
LPH†	Load high P register	1	0 1 0 1 0 0 1 1 I ◄——D——►
LT	Load T register	1	0 0 1 1 1 1 0 0 I ◄——D——►
LTA	Load T register and accumulate previous product	1	0 0 1 1 1 1 0 1 I ◄——D——►
LTD	Load T register, accumulate previous product, and move data	1	0 0 1 1 1 1 1 1 I ◄——D——►
LTP†	Load T register and store P register in accumulator	1	0 0 1 1 1 1 1 0 I ◄——D——►
LTS†	Load T register and subtract previous product	1	0 1 0 1 1 0 1 1 I ◄——D——►
MAC†	Multiply and accumulate	2	0 1 0 1 1 1 0 1 I ◄——D——►
MACD†	Multiply and accumulate with data move	2	0 1 0 1 1 1 0 0 I ◄——D——►
MPY	Multiply (with T register, store product in P register)	1	0 0 1 1 1 0 0 0 I ◄——D——►
MPYA‡	Multiply and accumulate previous product	1	0 0 1 1 1 0 1 0 I ◄——D——►
MPYK	Multiply immediate	1	1 0 1 ◄——K——►
MPYS‡	Multiply and subtract previous product	1	0 0 1 1 1 0 1 1 I ◄——D——►
MPYU‡	Multiply unsigned	1	1 1 0 0 1 1 1 1 I ◄——D——►
PAC	Load accumulator with P register	1	1 1 0 0 1 1 1 0 0 0 0 1 0 1 0 0
SPAC	Subtract P register from accumulator	1	1 1 0 0 1 1 1 0 0 0 0 1 0 1 1 0
SPH‡	Store high P register	1	0 1 1 1 1 1 0 1 I ◄——D——►
SPL‡	Store low P register	1	0 1 1 1 1 1 0 0 I ◄——D——►
SPM†	Set P register output shift mode	1	1 1 0 0 1 1 1 0 0 0 0 0 1 0 ◄PM►
SQRA†	Square and accumulate	1	0 0 1 1 1 0 0 1 I ◄——D——►
SQRS†	Square and subtract previous product	1	0 1 0 1 1 0 1 0 I ◄——D——►

†These instructions are not included in the TMS32010 instruction set.
‡These instructions are not included in the TMS32020 instruction set.

TABLE 2. TMS320C26 INSTRUCTION SET SUMMARY (CONTINUED)

BRANCH/CALL INSTRUCTIONS																			
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE																
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	Branch unconditionally	2	1	1	1	1	1	1	1	1	1	←D→						
BACC†	Branch to address specified by accumulator	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	0	1
BANZ	Branch on auxiliary register not zero	2	1	1	1	1	1	0	1	1	1	←D→						
BBNZ†	Branch if TC bit ≠ 0	2	1	1	1	1	1	0	0	1	1	←D→						
BBZ†	Branch if TC bit = 0	2	1	1	1	1	1	0	0	0	1	←D→						
BC‡	Branch on carry	2	0	1	0	1	1	1	1	0	1	←D→						
BGEZ	Branch if accumulator ≥ 0	2	1	1	1	1	0	1	0	0	1	←D→						
BGZ	Branch if accumulator > 0	2	1	1	1	1	0	0	0	1	1	←D→						
BIOZ	Branch on I/O status = 0	2	1	1	1	1	1	0	1	0	1	←D→						
BLEZ	Branch if accumulator ≤ 0	2	1	1	1	1	0	0	1	0	1	←D→						
BLZ	Branch if accumulator < 0	2	1	1	1	1	0	0	1	1	1	←D→						
BNC‡	Branch on no carry	2	0	1	0	1	1	1	1	1	1	←D→						
BNV†	Branch if no overflow	2	1	1	1	1	0	1	1	1	1	←D→						
BNZ	Branch if accumulator ≠ 0	2	1	1	1	1	0	1	0	1	1	←D→						
BV	Branch on overflow	2	1	1	1	1	0	0	0	0	1	←D→						
BZ	Branch if accumulator = 0	2	1	1	1	1	0	1	1	0	1	←D→						
CALA	Call subroutine indirect	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	0	0
CALL	Call subroutine	2	1	1	1	1	1	1	1	0	1	←D→						
RET	Return from subroutine	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	1	0

I/O AND DATA MEMORY OPERATIONS																			
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE																
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLKD†	Block move from data memory to data memory	2	1	1	1	1	1	1	0	1	I	←D→						
BLKP†	Block move from program memory to data memory	2	1	1	1	1	1	1	0	0	I	←D→						
DMOV	Data move in data memory	1	0	1	0	1	0	1	1	0	I	←D→						
FORT†	Format serial port registers	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	1	1	FO
IN	Input data from port	1	1	0	0	0	←PA→				I	←D→							
OUT	Output data to port	1	1	1	1	0	←PA→				I	←D→							
RFSM‡	Reset serial port frame synchronization mode	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	1	0
RTXM†	Reset serial port transmit mode	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0
RXF†	Reset external flag	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	0
SFSM‡	Set serial port frame synchronization mode	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	1	1
STXM†	Set serial port transmit mode	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	0	1
SXF†	Set external flag	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1
TBLR	Table read	1	0	1	0	1	1	0	0	0	I	←D→						
TBLW	Table write	1	0	1	0	1	1	0	0	1	I	←D→						

† These instructions are not included in the TMS32010 instruction set.
‡ These instructions are not included in the TMS32020 instruction set.

TABLE 2. TMS320C26 INSTRUCTION SET SUMMARY (CONCLUDED)

CONTROL INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT†	Test bit	1	1	0	0	1	◄	—	B	—	►	I	◄	—	—	D	—	►
BITT†	Test bit specified by T register	1	0	1	0	1	0	1	1	1	I	◄	—	—	—	D	—	►
CONF0#	Configure all blocks as Data	1	1	1	0	0	1	1	1	0	0	0	1	1	1	1	0	0
CONF1#	Configure block B0 as program	1	1	1	0	0	1	1	1	0	0	0	1	1	1	1	0	1
CONF2#	Configure blocks B0 and B1 as program	1	1	1	0	0	1	1	1	0	0	0	1	1	1	1	1	0
CONF3#	Configure blocks B0, B1 and B3 as program	1	1	1	0	0	1	1	1	0	0	0	1	1	1	1	1	1
DINT	Disable interrupt	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1
EINT	Enable interrupt	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
IDLE†	Idle until interrupt	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	1
LST	Load status register ST0	1	0	1	0	1	0	0	0	0	I	◄	—	—	—	D	—	►
LST1†	Load status register ST1	1	0	1	0	1	0	0	0	1	I	◄	—	—	—	D	—	►
NOP	No operation	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
POP	Pop top of stack to low accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	0	1
POPD†	Pop top of stack to data memory	1	0	1	1	1	1	0	1	0	I	◄	—	—	—	D	—	►
PSHD†	Push data memory value onto stack	1	0	1	0	1	0	1	0	0	I	◄	—	—	—	D	—	►
PUSH	Push low accumulator onto stack	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	0	0
RC‡	Reset carry bit	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	0	0
RHM‡	Reset hold mode	1	1	1	0	0	1	1	1	0	0	0	1	1	1	0	0	0
ROVM	Reset overflow mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1	0
RPT†	Repeat instruction as specified by data memory value	1	0	1	0	0	1	0	1	1	I	◄	—	—	—	D	—	►
RPTK†	Repeat instruction as specified by immediate value	1	1	1	0	0	1	0	1	1	◄	—	—	—	—	K	—	►
RSXM†	Reset sign-extension mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	1	0
RTC‡	Reset test/control flag	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	0	1	0
SC‡	Set carry bit	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	0	0	1
SHM‡	Set hold mode	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	0	0	1
SOVM	Set overflow mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1
SST	Store status register ST0	1	0	1	1	1	1	0	0	0	I	◄	—	—	—	D	—	►
SST1†	Store status register ST1	1	0	1	1	1	1	0	0	1	I	◄	—	—	—	D	—	►
SSXM†	Set sign-extension mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1	1	1
STC‡	Set test/control flag	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	1	1
TRAP†	Software interrupt	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0

† These instructions are not included in the TMS32010 instruction set.
‡ These instructions are not included in the TMS32020 instruction set.
# These instructions are not included in the TMS320C25 instruction set.

development systems and software support

TEXAS INSTRUMENTS offers concentrated development support and complete documentation for designing a TMS320C26 based microprocessor system. When developing an application, tools are provided to evaluate the performance of the processor, to develop the algorithm implementation, and to fully integrate the design's software and hardware modules. When questions arise, additional support can be obtained by calling the nearest Texas Instruments Regional Technology Center (RTC).

Sophisticated development operations are performed with the TMS320C26 Macro Assembler Linker Simulator, and Emulator (XDS). The macro assembler and linker are used to translate program modules into object code and link them together. This puts the program modules into a form which can be loaded into the TMS320C26 Simulator or Emulator. The simulatore provides a quick means for initially debugging TMS320C26 software while the emulator provides the real time in circuit emulation necessary to perform system level debug efficiently.

Table 3 gives a complete list of TMS320C26 software and hardware developments tools

TABLE 3. TMS320C26 SOFTWARE AND HARDWARE SUPPORT

MACRO ASSEMBLERS/LINKER		
HOST COMPUTER	OPERATING SYSTEMS	PART NUMBER
DEC VAX	VMS	TMDS3242250-08
IBM PC	MS/PC-DOS	TMDS3242850-02
SIMULATORS		
HOST COMPUTER	OPERATING SYSTEMS	PART NUMBER
DEC VAX	VMS	TMDS3242251-08
IBM PC	MS/PC-DOS	TMDS3242851-02
EMULATORS		
MODEL	POWER SUPPLY	PART NUMBER
XDS/22	INCLUDED	TMDS3262292

Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication "Guidelines for Handling Electrostatic-Discharge Sensitive (ESDS) Devices and Assemblies" available from Texas Instruments.

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}‡ . . . . . −0.3 V to 7 V
Input voltage range . . . . . −0.3 V to 7 V
Output voltage range . . . . . −0.3 V to 7 V
Continuous power dissipation . . . . . 1.5 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC} Supply voltage		4.75	5	5.25	V
V_{SS} Supply voltage			0		V
V_{IH} High-level input voltage	All inputs except CLKIN/CLKX/CLKR / $\overline{INT}$ (0 - 2)	2.35		V_{CC}+0.3	V
	$\overline{INT}$ (0 - 2)	2.5		V_{CC}+0.3	V
	CLKIN/CLKX/CLKR	3.5		V_{CC}+0.3	V
V_{IL} Low-level input voltage	All inputs except CLKIN	−0.3		0.8	V
	CLKIN	−0.3		0.8	V
I_{OH} High-level output current				300	μA
I_{OL} Low-level output current				2	mA
T_A Operating free-air temperature		0		70	°C

electrical characteristics over specified free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH} High-level output voltage		V_{CC} = MIN, I_{OH} = MAX	2.4	3		V
V_{OL} Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX		0.3	0.6	V
I_Z Three-state current		V_{CC} = MAX	−20		20	μA
I_I Input current		V_I = V_{SS} to V_{CC}	−10		10	μA
I_{CC} Supply current	Normal	T_A = 0°C, V_{CC} = MAX, f_x = MAX		110	220	mA
	Idle/$\overline{HOLD}$			70	100	
C_I Input capacitance				15		pF
C_O Output capacitance				15		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

CLOCK CHARACTERISTICS AND TIMING

The TMS320C26 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 2). The frequency of CLKOUT1 is one-fourth the crystal fundamental frequency. The crystal should be either fundamental or overtone mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF. Note that overtone crystals require an additional tuned LC circuit (see the application report, *Hardware Interfacing to the TMS320C25).*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_x	Input clock frequency	T_A = 0°C to 70°C	6.7		40.96	MHz
f_{sx}	Serial port frequency	T_A = 0°C to 70°C	0		5,120	kHz
C1, C2		T_A = 0°C to 70°C		10		pF

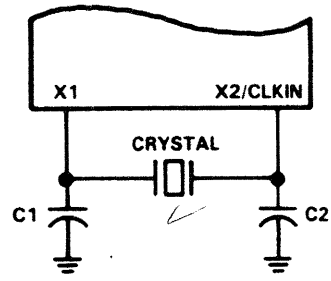


FIGURE 2. INTERNAL CLOCK OPTION

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the following table.

switching characteristics over recommended operating conditions (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(C)}$	CLKOUT1/CLKOUT2 cycle time	97.7		597	ns
$t_{d(CIH-C)}$	CLKIN high to CLKOUT1/CLKOUT2/$\overline{STRB}$ high/low	5		30	ns
$t_{f(C)}$	CLKOUT1/CLKOUT2/$\overline{STRB}$ fall time			5	ns
$t_{r(C)}$	CLKOUT1/CLKOUT2/$\overline{STRB}$ rise time			5	ns
$t_{w(CL)}$	CLKOUT1/CLKOUT2 low pulse duration	2Q−8	2Q	2Q+8	ns
$t_{w(CH)}$	CLKOUT1/CLKOUT2 high pulse duration	2Q−8	2Q	2Q+8	ns
$t_{d(C1-C2)}$	CLKOUT1 high to CLKOUT2 low, CLKOUT2 high to CLKOUT1 high, etc.	Q−5	Q	Q+5	ns

NOTE 3: Q = $1/4t_{c(C)}$.

timing requirements over recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$t_{c(CI)}$	CLKIN cycle time	24.4		150	ns
$t_{f(CI)}$	CLKIN fall time			5	ns
$t_{r(CI)}$	CLKIN rise time			5	ns
$t_{w(CIL)}$	CLKIN low pulse duration, $t_{c(CI)}$ = 50 ns (see Note 4)	5		20	ns
$t_{w(CIH)}$	CLKIN high pulse duration, $t_{c(CI)}$ = 50 ns (see Note 4)	5		20	ns
$t_{su(S)}$	$\overline{SYNC}$ setup time before CKLIN low	5		Q−5	ns
$t_{h(S)}$	$\overline{SYNC}$ hold time from CLKIN low	8			ns

NOTES: 3. Q = $1/4t_{c(C)}$.
4. CLKIN duty cycle $[t_{r(CI)} + t_{w(CIH)}]/t_{c(CI)}$ must be within 40-60%.

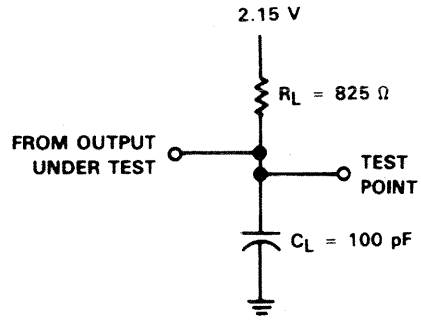
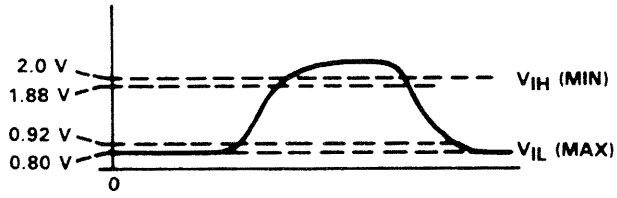
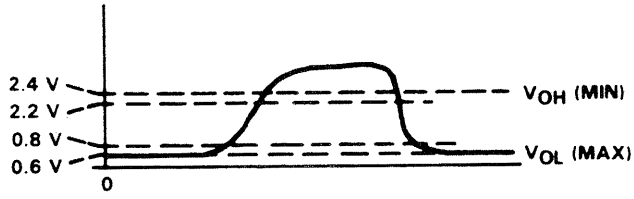


FIGURE 3. TEST LOAD CIRCUIT



(a) INPUT



(b) OUTPUTS

FIGURE 4. VOLTAGE REFERENCE LEVELS

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(C1-S)}$	$\overline{STRB}$ from CLKOUT1 (if $\overline{STRB}$ is present)	Q−6	Q	Q+6	ns
$t_{d(C2-S)}$	CLKOUT2 to $\overline{STRB}$ (if $\overline{STRB}$ is present)	−6	0	6	ns
$t_{su(A)}$	Address setup time before $\overline{STRB}$ low (see Note 5)	Q−12			ns
$t_{h(A)}$	Address hold time after $\overline{STRB}$ high (see Note 5)	Q−8			ns
$t_{w(SL)}$	$\overline{STRB}$ low pulse duration (no wait states, see Note 6)		2Q		ns
$t_{w(SH)}$	$\overline{STRB}$ high pulse duration (between consecutive cycles, see Note 6)		2Q		ns
$t_{su(D)W}$	Data write setup time before $\overline{STRB}$ high (no wait states)	2Q−20			ns
$t_{h(D)W}$	Data write hold time from $\overline{STRB}$ high	Q−10	Q		ns
$t_{en(D)}$	Data bus starts being driven after $\overline{STRB}$ low (write cycle)	0			ns
$t_{dis(D)}$	Data bus three-state after $\overline{STRB}$ high (write cycle)		Q	Q+15	ns
$t_{d(MSC)}$	$\overline{MSC}$ valid from CLKOUT1	−12	0	12	ns

NOTES: 3. Q = $1/4t_{c(C)}$.
5. A15-A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as "address."
6. Delays between CLKOUT1/CLKOUT2 edges and $\overline{STRB}$ edges track each other, resulting in $t_{w(SL)}$ and $t_{w(SH)}$ being 2Q with no wait states.

timing requirements over recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$t_{a(A)}$	Read data access time from address time (read cycle, see Notes 5 and 7)			3Q−35	ns
$t_{su(D)R}$	Data read setup time before $\overline{STRB}$ high	23			ns
$t_{h(D)R}$	Data read hold time from $\overline{STRB}$ high	0			ns
$t_{d(SL-R)}$	READY valid after $\overline{STRB}$ low (no wait states)			Q−20	ns
$t_{d(C2H-R)}$	READY valid after CLKOUT2 high			Q−20	ns
$t_{h(SL-R)}$	READY hold time after $\overline{STRB}$ low (no wait states)	Q+3			ns
$t_{h(C2H-R)}$	READY hold after CLKOUT2 high	Q+3			ns
$t_{d(M-R)}$	READY valid after $\overline{MSC}$ valid			2Q−25	ns
$t_{h(M-R)}$	READY hold time after $\overline{MSC}$ valid	0			ns

NOTES: 3. Q = $1/4t_{c(C)}$.
5. A15-A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as "address."
7. Read data access time is defined as $t_{a(A)} = t_{su(A)} + t_{w(SL)} - t_{su(D)R}$.

$\overline{RS}$, $\overline{INT}$, $\overline{BIO}$, and XF TIMING

switching characteristics over recommended operating conditions (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(RS)}$	CLKOUT1 low to reset state entered			22	ns
$t_{d(IACK)}$	CLKOUT1 to $\overline{IACK}$ valid	−6	0	12	ns
$t_{d(XF)}$	XF valid before falling edge of $\overline{STRB}$	Q−15			ns

NOTES: 3. Q = $1/4t_{c(C)}$.
8. $\overline{RS}$, $\overline{INT}$, and $\overline{BIO}$ are asynchronous inputs and can occur at any time during a clock cycle. However, if the specified setup time is met, the exact sequence shown in the timing diagrams will occur.

timing requirements over recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$t_{su(IN)}$	$\overline{INT}/\overline{BIO}/\overline{RS}$ setup before CLKOUT1 high	32			ns
$t_{h(IN)}$	$\overline{INT}/\overline{BIO}/\overline{RS}$ hold after CLKOUT1 high	0			ns
$t_{f(IN)}$	$\overline{INT}/\overline{BIO}$ fall time			8	ns
$t_{w(IN)}$	$\overline{INT}/\overline{BIO}$ low pulse duration	$t_{c(C)}$			ns
$t_{w(RS)}$	$\overline{RS}$ low pulse duration	$3t_{c(C)}$			ns

NOTES: 3. $Q = 1/4t_{c(C)}$.
8. $\overline{RS}$, $\overline{INT}$, and $\overline{BIO}$ are asynchronous inputs and can occur at any time during a clock cycle. However, if the specified setup time is met, the exact sequence shown in the timing diagrams will occur.

$\overline{HOLD}$ TIMING

switching characteristics over recommended operating conditions (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(C1L-AL)}$	$\overline{HOLDA}$ low after CLKOUT1 low	0		10	ns
$t_{dis(AL-A)}$	$\overline{HOLDA}$ low to address three-state		0		ns
$t_{dis(C1L-A)}$	Address three-state after CLKOUT1 low ($\overline{HOLD}$ mode, see Note 9)			20	ns
$t_{d(HH-AH)}$	$\overline{HOLD}$ high to $\overline{HOLDA}$ high			25	ns
$t_{en(A-C1L)}$	Address driven before CLKOUT1 low ($\overline{HOLD}$ mode, see Note 9)			8	ns

NOTES: 3. $Q = 1.4t_{c(C)}$.
9. A15-A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, $\overline{STRB}$, and R/$\overline{W}$ timings are all included in timings referenced as "address."

timing requirements over recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$t_{d(C2H-H)}$	$\overline{HOLD}$ valid after CLKOUT2 high			Q – 24	ns

NOTE 3: $Q = 1/4t_{c(C)}$.

SERIAL PORT TIMING

switching characteristics over recommended operating conditions (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CH-DX)}$	DX valid after CLKX rising edge (see Note 10)			75	ns
$t_{d(FL-DX)}$	DX valid after FSX falling edge (TXM = 0, see Note 10)			40	ns
$t_{d(CH-FS)}$	FSX valid after CLKX rising edge (TXM = 1)			40	ns

NOTES: 3. $Q = 1/4t_{c(C)}$.
10. The last occurrence of FSX falling and CLKX rising.

timing requirements over recommended operating conditions (see Note 3)

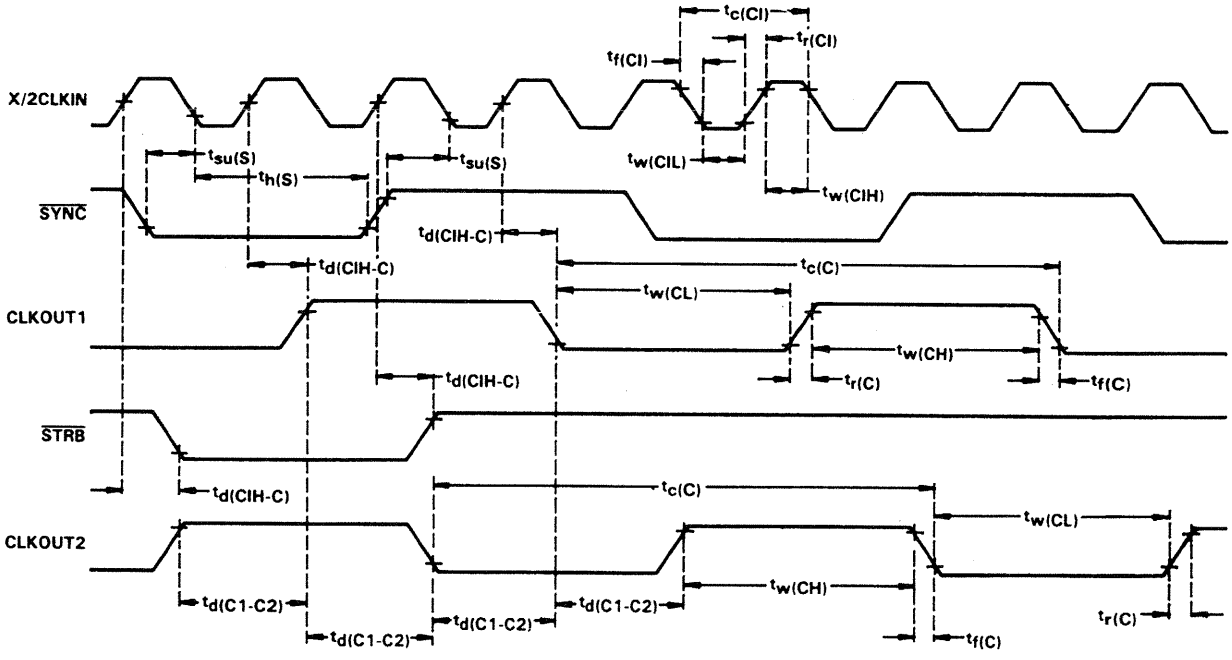
		MIN	NOM	MAX	UNIT
$t_{c(SCK)}$	Serial port clock (CLKX/CLKR) cycle time	200			ns
$t_{f(SCK)}$	Serial port clock (CLKX/CLKR) fall time			25	ns
$t_{r(SCK)}$	Serial port clock (CLKX/CLKR) rise time			25	ns
$t_{w(SCK)}$	Serial port clock (CLKX/CLKR) low pulse duration (see Note 11)	80			ns
$t_{w(SCK)}$	Serial port clock (CLKX/CLKR) high pulse duration (see Note 11)	80			ns
$t_{su(FS)}$	FSX/FSR setup time before CLKX/CLKR falling edge (TXM = 0)	18			ns
$t_{h(FS)}$	FSX/FSR hold time after CLKX/CLKR falling edge (TXM = 0)	20			ns
$t_{su(DR)}$	DR setup time before CLKR falling edge	10			ns
$t_{h(DR)}$	DR hold time after CLKR falling edge	20			ns

NOTES: 3. $Q = 1/4t_{c(C)}$.
11. The duty cycle of the serial port clock must be within 40-60%.

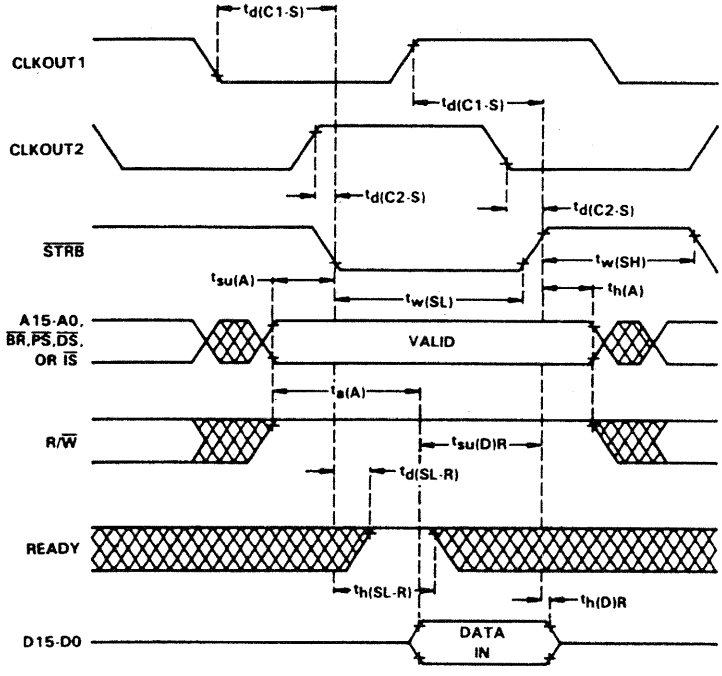
TIMING DIAGRAMS

Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

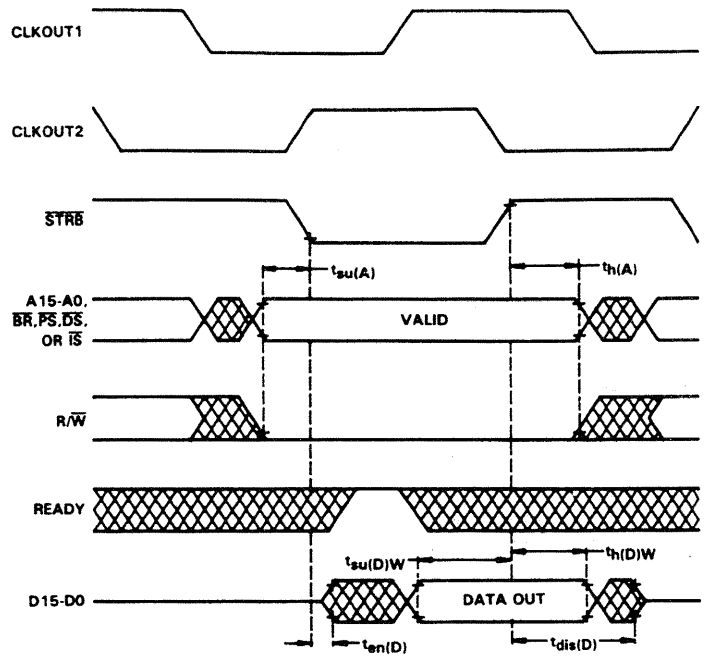
clock timing



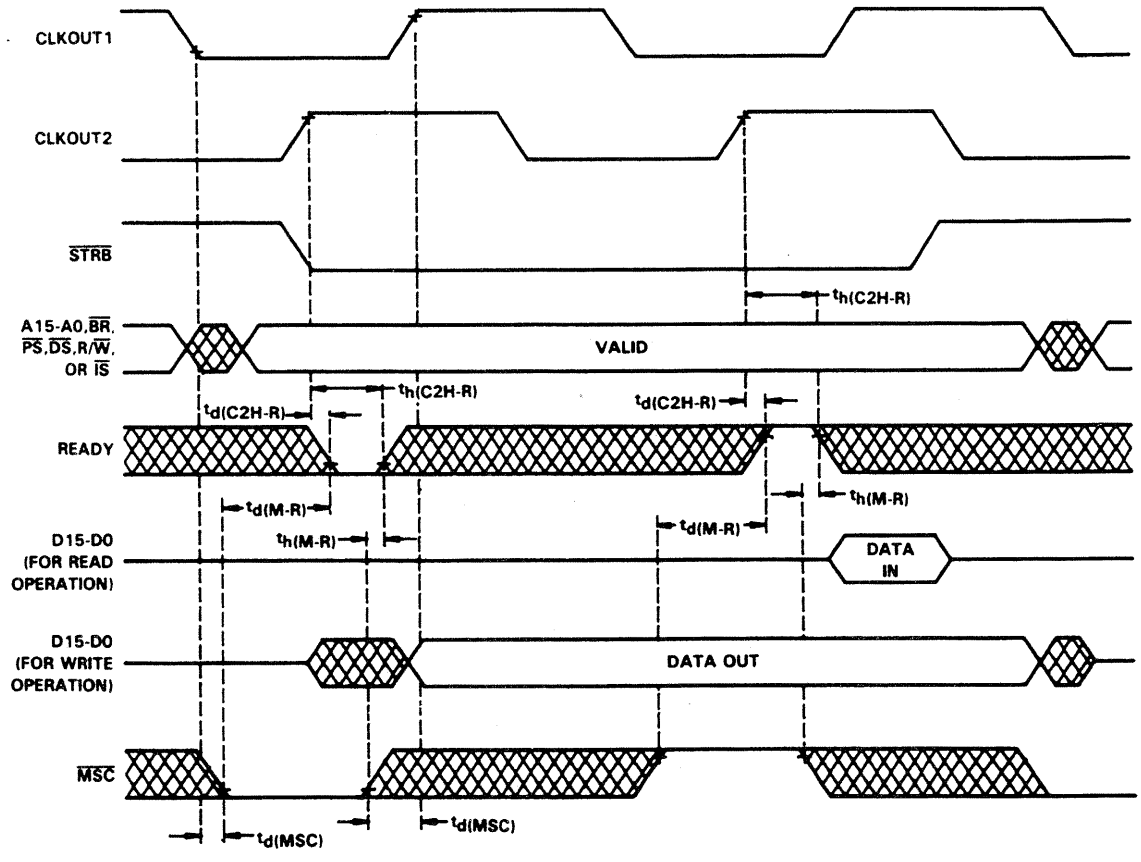
memory read timing



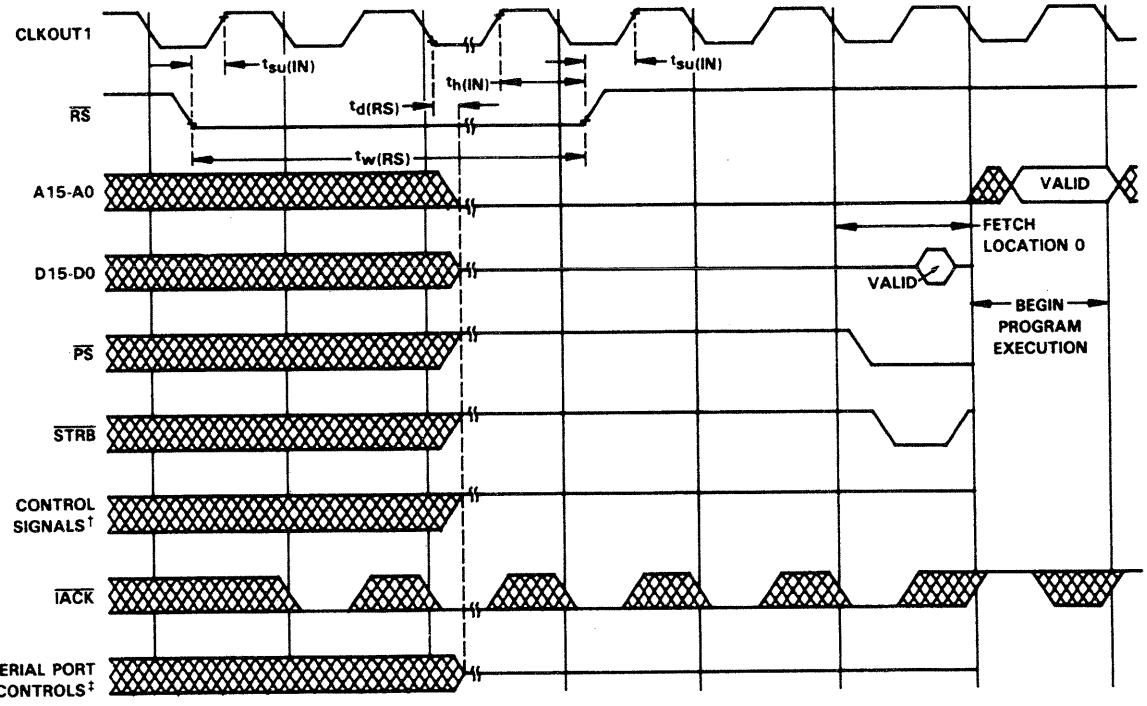
memory write timing



one wait-state memory access timing

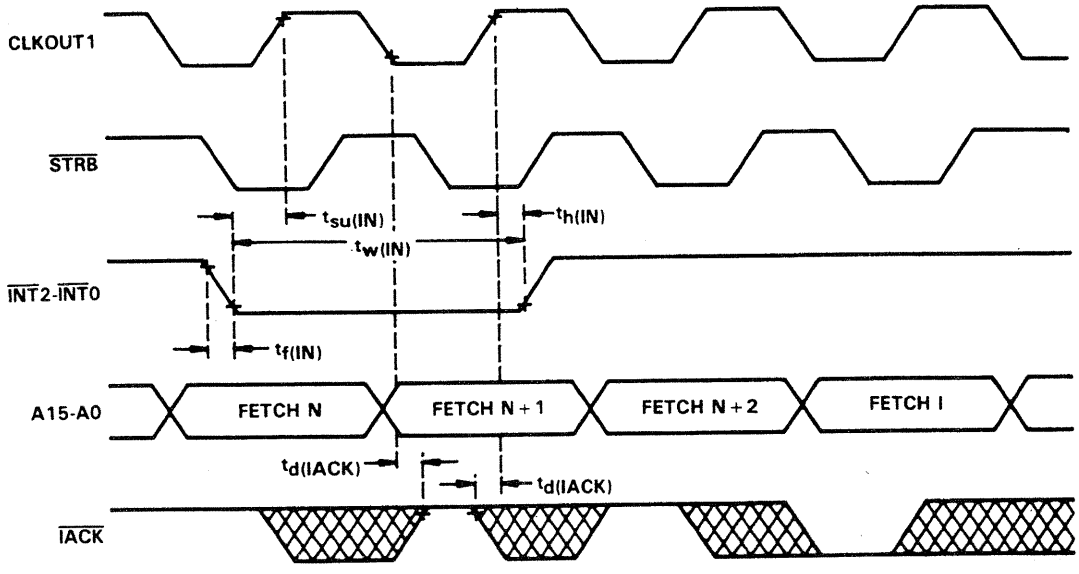


reset timing

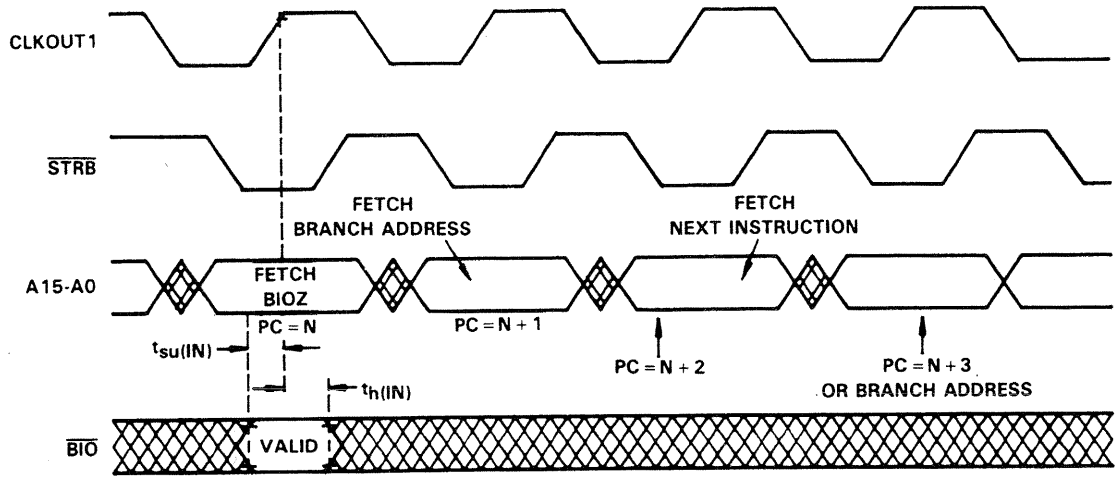


†Control signals are $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and XF.
‡Serial port controls are DX and FSX.

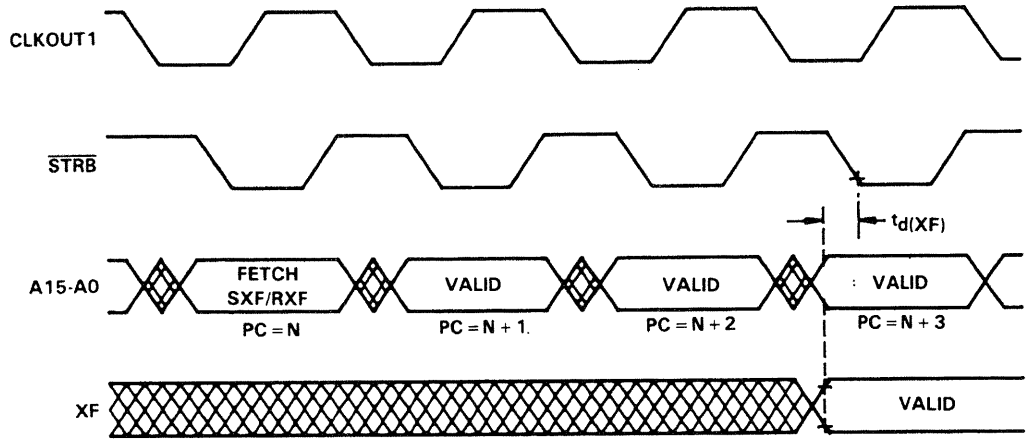
interrupt timing



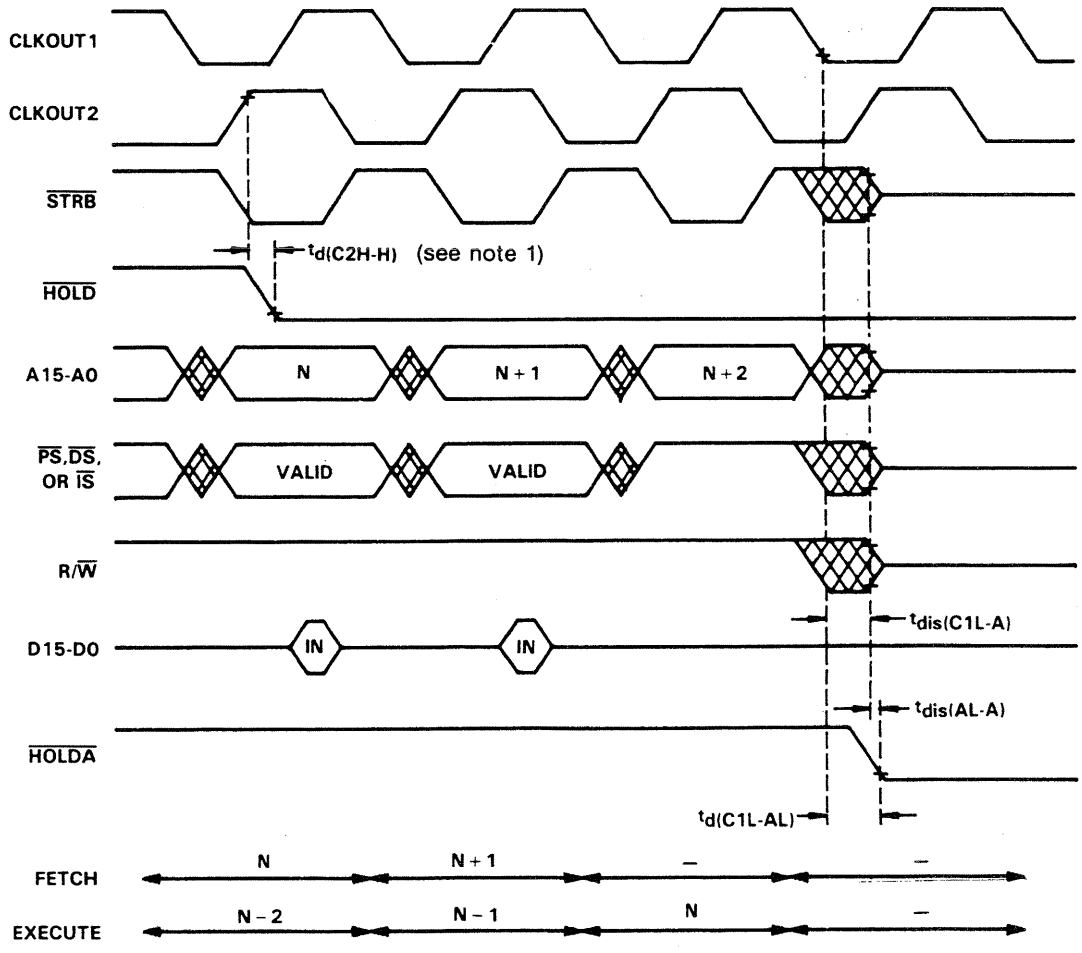
$\overline{\text{BIO}}$ timing



external flag timing



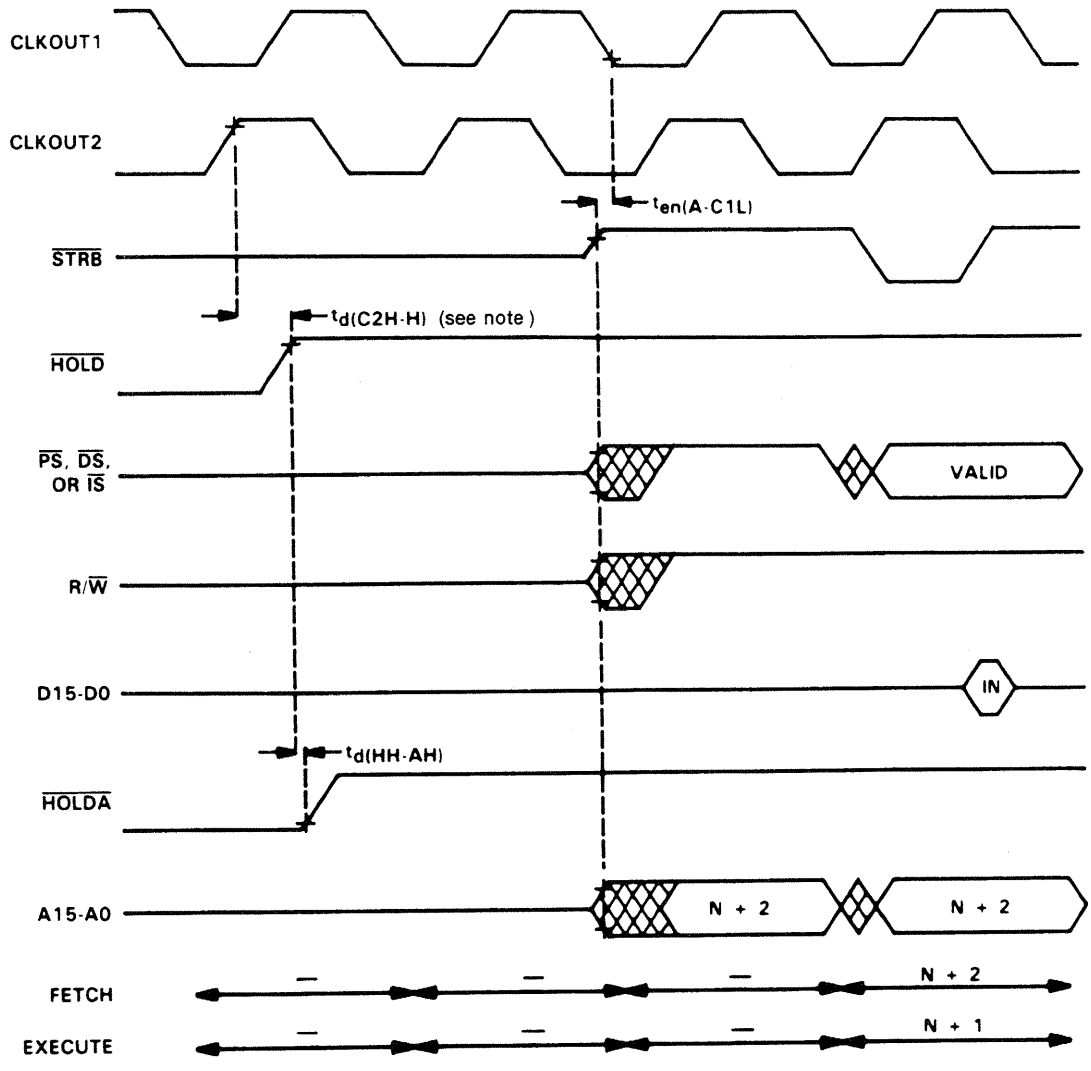
$\overline{\text{HOLD}}$ timing (part A)



NOTE 1:

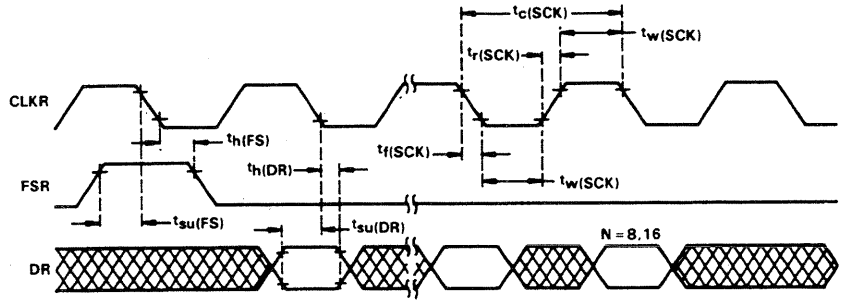
"$\overline{\text{HOLD}}$ is an asynchronous input can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur; otherwise, a delay of one CLKOUT2 cycle will occur."

$\overline{\text{HOLD}}$ timing (part B)

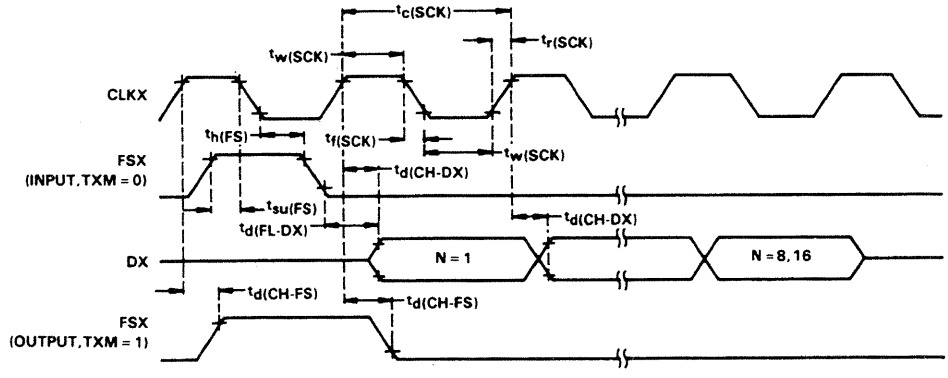


Note: $\overline{\text{HOLD}}$ is an asynchronous input and can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur; otherwise a delay of one CLKOUT2 cycle will occur.

serial port receive timing

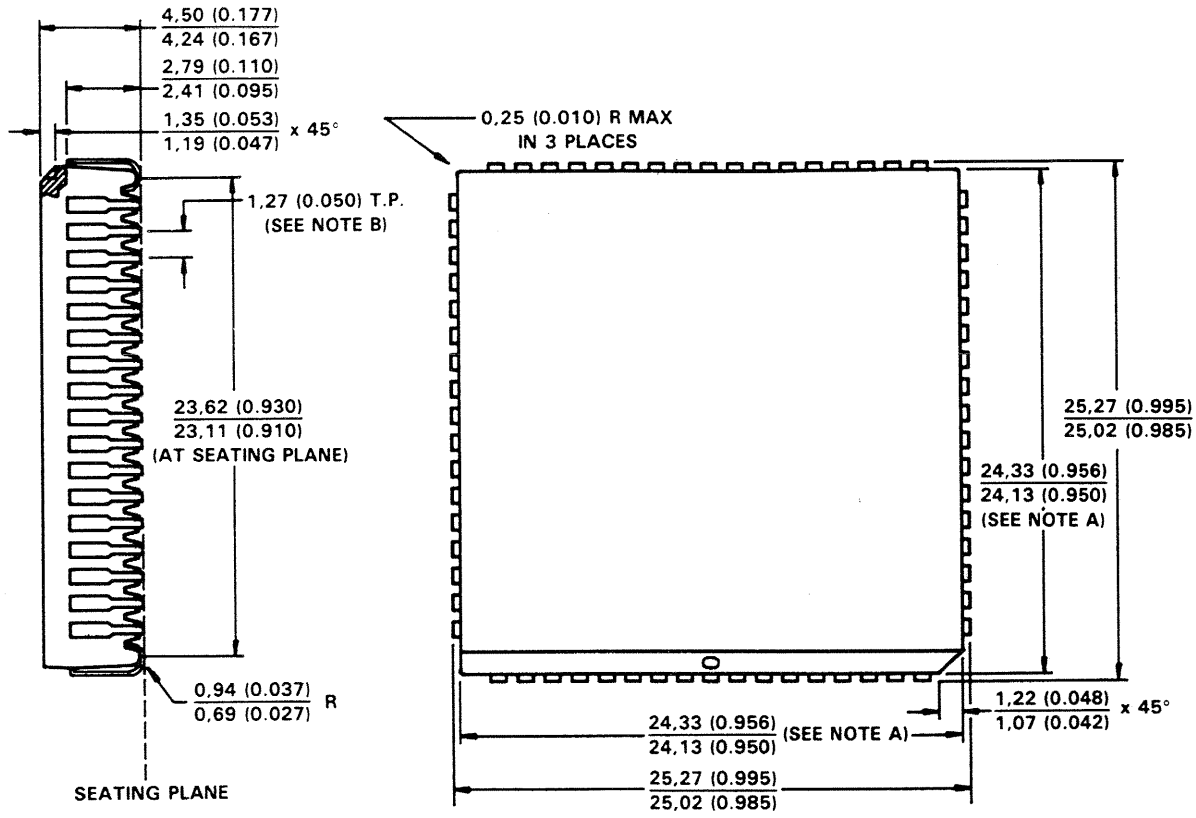


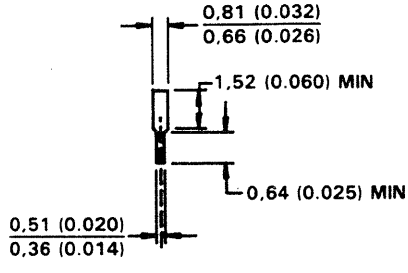
serial port transmit timing



MECHANICAL DATA

68-pin plastic leaded chip carrier package





LEAD DETAIL

THERMAL RESISTANCE CHARACTERISTICS

PARAMETER		MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	46	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	11	°C/W

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by this dimension.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.