intel®

2911A
PCM CODEC — A LAW
8-BIT COMPANDED A/D AND D/A CONVERTER

2911A-1	Microcomputer* Mode or Direct Mode
2911A-2	Direct Mode Only

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G732 Compatible, Even Order Bits Inversion Included**
- **Microcomputer Interface with On-Chip Time-Slot Computation (2911A-1)**
- **Simple Direct Mode Interface When Fixed Timeslots Are Used**
- **66 dB Dynamic Range, with Resolution Equivalent to 11-Bit Linear Conversion Around Zero**
- **±5% Power Supplies: +12V, +5V, −5V**
- **Precision On-Chip Voltage Reference**
- **Low Power Consumption 230 mW Typ. Standby Power 33 mW Typ.**
- **Fabricated with Reliable N-Channel MOS Process**

The Intel® 2911A is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link.

The primary applications are in telephone systems:

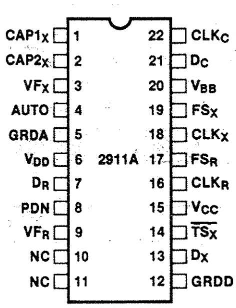
- Transmission — 30/32 Channel Systems at 2.048 Mbps
- Switching — Digital PBX's and Central Office Switching Systems
- Concentration — Subscriber Carrier/Concentrators

The wide dynamic range of the 2911A (66 dB) and the minimal conversion time (80 μsec minimum) make it an ideal product for other applications, like:

- Data Acquisition
- Secure Communications Systems
- Telemetry
- Signal Processing Systems

*Microcomputer mode is explained on page 4.

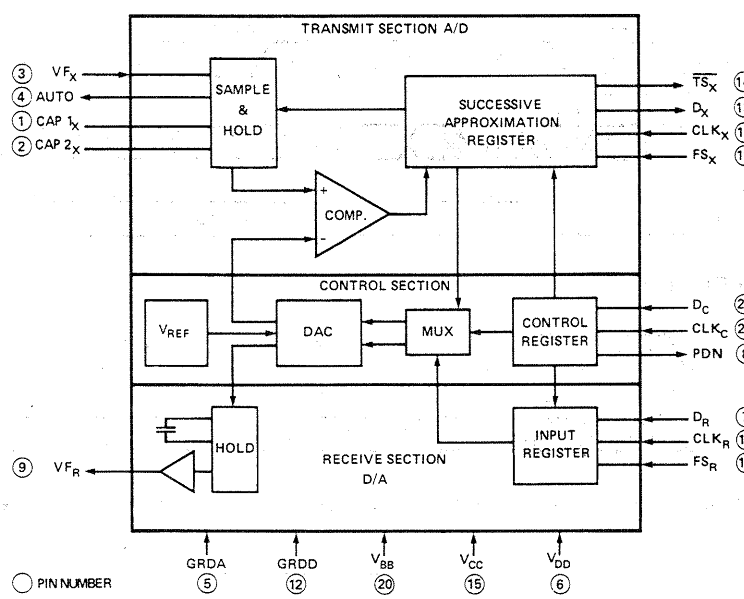
PIN CONFIGURATION



PIN NAMES

CAP 1_X, CAP 2_X	Holding Capacitor
VF_X	Analog Input
VF_R	Analog Output
D_R, D_C	Digital Input
D_X, $\overline{TS}_X$	Digital Output
CLK_C, CLK_X, CLK_R	Clock Input
FS_X, FS_R	Frame Sync Input
AUTO	Auto Zero Output
V_{BB}	Power (−5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
PDN	Power Down
GRDA	Analog Ground
GRDD	Digital Ground
NC	No Connect

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Function	Description
1	$CAP1_X$	Hold	Connections for the transmit holding capacitor. Refer to Applications section.
2	$CAP2_X$		
3	VF_X	Input	Analog input to be encoded into a PCM word. The signal on this lead is sampled at the same rate as the transmit frame synchronization pulse FS_X, and the sample value is held in the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads until the encoding process is completed.
4	AUTO	Output	Most significant bit of the encoded PCM word (+5V for negative, −5V for positive values). Refer to the Codec Applications section.
5	GRDA	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally.
6	V_{DD}	Power	+12V±5%; referenced to GRDA.
7	D_R	Input	Receive PCM highway (serial bus) interface. The Codec serially receives a PCM word (8 bits) through this lead at the proper time defined by FS_R, CLK_R, D_C, and CLK_C.
8	PDN	Output	Active high when the Codec is in the power down mode. TTL interface. Open drain output.
9	VF_R	Output	Analog Output. The voltage present on VF_R is the decoded value of the PCM word received on lead D_R. This value is held constant between two conversions.
10	NC	No Connects	Recommended practice is to strap these NC's to GRDA.
11	NC		
12	GRDD	Ground	Ground return common to the logic power supply; V_{CC}.
13	D_X	Output	Output of the transmit side onto the send PCM highway (serial bus). The 8-bit PCM word is serially sent out on this pin at the proper time defined by FS_X, CLK_X, D_C, and CLK_C. TTL three-state output.

Pin No.	Symbol	Function	Description
14	$\overline{TS_X}$	Output	Normally high, this signal goes low while the Codec is transmitting an 8-bit PCM word on the D_X lead. (Timeslot information used for diagnostic purposes and also to gate the data on the D_X lead.) TTL interface, open drain output.
15	V_{CC}	Power	+5V±5%, referenced to GRDD.
16	CLK_R	Input	Master receive clock defining the bit rate on the receive PCM highway. Typically 2.048 Mbps for a carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL compatible.
17	FS_R	Input	Frame synchronization pulse for the receive PCM highway. Resets the on-chip timeslot counter for the receive side. Maximum repetition rate 12 KHz. TTL interface.
18	CLK_X	Input	Master transmit clock defining the bit rate on the transmit PCM highway. Typically 2.048 Mbps for a carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL interface.
19	FS_X	Input	Frame synchronization pulse for the transmit PCM highway. Resets the on-chip timeslot counter for the transmit side. Maximum repetition rate 12 KHz. TTL interface.
20	V_{BB}	Power	−5V±5%, referenced to GRDA.
21	D_C	Input	Data input to program the Codec for the chosen mode of operation. Becomes an active low chip select when CLK_C is tied to V_{CC}. TTL interface.
22	CLK_C	Input	Clock input to clock in the data on the D_C lead when the timeslot assignment feature is used; tied to V_{CC} to disable this feature. TTL interface.

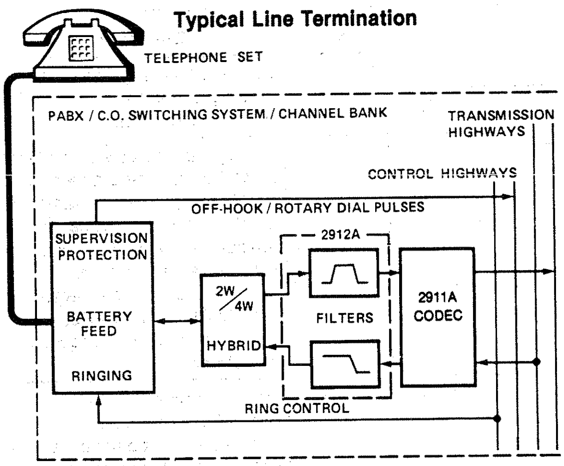
FUNCTIONAL DESCRIPTION

The 2911A PCM Codec provides the analog-to-digital and the digital-to-analog conversions necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. The Codec is intended to be used on line and trunk terminations.

In a typical telephone system the Codec is located between the PCM highways and the channel filters.

The Codec encodes the incoming analog signal at the frame rate (FS_X) into an 8-bit PCM word which is sent out on the D_X lead at the proper time. Similarly, on the receive link, the Codec fetches an 8-bit PCM word from the receive highway (D_R lead) and decodes an analog value which will remain constant on lead VF_R until the next receive frame. Transmit and receive frames are independent. They can be asynchronous (transmission) or synchronous (switching) with each other.

Circuitry is provided within the Codec to internally define the transmit and receive timeslots. In small systems this may eliminate the need for any external timeslot exchange; in large systems it provides one level of concentration. This feature can be bypassed and discrete timeslots sent to each Codec within a system.



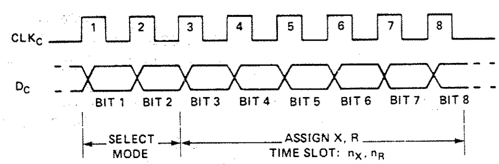
Functional Block Diagram of Line Circuit

In the power-down mode, most functions of the Codec are directly disabled to reduce power dissipation to a minimum.

CODEC OPERATION

Codec Control

The operation of the 2911A is defined by serially loading an 8-bit word through the D_C lead (data) and the CLK_C lead (clock). The loading is asynchronous with the other operations of the Codec, and takes place whenever transitions occur on the CLK_C lead. The D_C input is loaded in during the trailing edge of the CLK_C input.



The control word contains two fields:

Bit 1 and Bit 2 define whether the subsequent 6 bits apply to both the transmit and receive side (00), the transmit side only (01), the receive side only (10), or whether the Codec should go into the standby, power-down mode (11). In the last case (11), the following 6 bits are irrelevant.

The last 6 bits of the control word define the timeslot assignment, from 000000 (timeslot 1) to 111111 (timeslot 64). Bit 3 is the most significant bit and bit 8 the least significant bit and last into the Codec.

Bit 1	Bit 2	Mode
0	0	X & R
0	1	X
1	0	R
1	1	Standby

Bit						
3	4	5	6	7	8	Time-Slot
0	0	0	0	0	0	1
0	0	0	0	0	1	2
•						•
•						•
•						•
•						•
1	1	1	1	1	1	64

The Codec will retain the control word (or words) until a new word is loaded in or until power is lost. This feature permits dynamic allocation of timeslots for switching applications.

Microcomputer Control Mode (2911A-1)

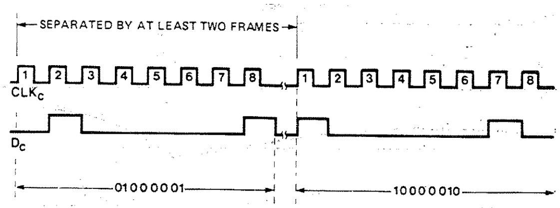
In the microcomputer mode, each Codec performs its own timeslot computation independently for the transmit and receive channels by counting clock pulses (CLK_X and CLK_R). All Codecs tied to the same data bus receive identical framing pulses (FS_X and FS_R). The framing pulses reset the on-chip timeslot counters every frame; hence the timeslot counters of all devices are synchronized. Each Codec is programmed via CLK_C and D_C for the desired transmit and receive timeslots according to the description in the Codec Control Section. All Codecs tied to the same D_R bus will, in general, have different receive timeslots, although that is not a device requirement. There may be separate busses for transmit and receive or all Codecs may transmit and receive over the same bus, in which case the transmit and receive channels must be synchronous ($CLK_X = CLK_R$). There are no other restrictions on timeslot assignments; a device may have the same transmit and receive timeslot even if a single bus is used.

There are several requirements for using the CLK_C-D_C interface in the microcomputer mode.

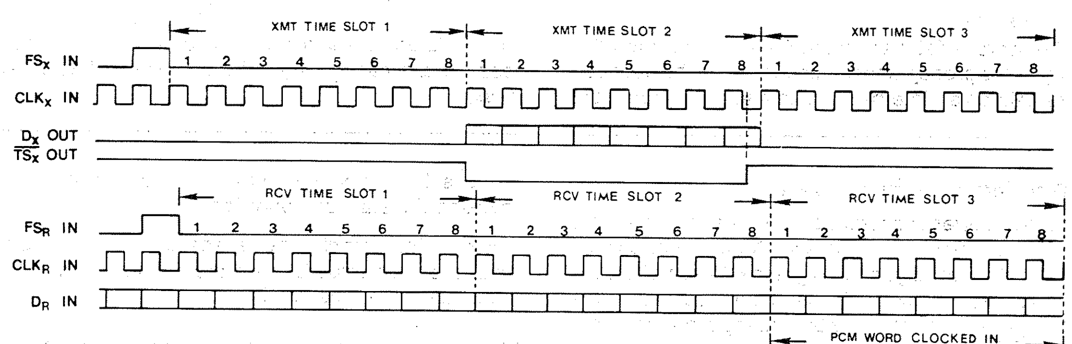
1. A complete timeslot assignment, consisting of eight negative transitions of CLK_C, must be made in less than one frame period. The assignment can overlap a framing pulse so long as all 8 control bits are clocked in within a total span of 125μsec (for an 8KHz frame rate). CLK_C must be left at a TTL low level when not assigning a timeslot.
2. A dead period of two frames must always be observed between successive timeslot assignments. The two frame delay is measured from the rising edge of the first CLK_C transition of the previous timeslot assigned.
3. When the device is in the power-down state a single control word will suffice to power-up the Codec and make a timeslot assignment. That is, the first assignment brings the device out of power-down and registers the timeslot information in the lower six bits of the control word.
4. Initialization sequence: The device contains an on-chip power-on clear function which guarantees that with proper sequencing of the supplies (V_{CC} or V_{DD} on last), the device will initialize with no timeslot assigned to either the transmit or receive channel. After a supply failure or whenever the supplies are applied, it is recommended that either power down assignment be made first, or the first timeslot assignment be a transmit timeslot or a transmit/receive timeslot. The consequence of making a receive timeslot assignment first, after supply application, is that the transmit channel will assume timeslot 1, potentially producing bus contention.
5. Transmit only/receive only operation is permitted provided that a power down assignment is made first. Otherwise, special circuits which use only one channel should be physically disconnected from the unused bus; this allows a timeslot to be made to an unused channel without consequence.

Example of Microcomputer Control Mode:

The two words 01000001 and 10000010 have been loaded into the Codec. The transmit side is now programmed for timeslot 2 and the receive side for timeslot 3. The Codec will output a PCM word on the transmit PCM highway (bus) during the timeslot 2 of the transmit frame, and will fetch a PCM word from the receive PCM highway during timeslot 3.



In this example the Codec interface to the PCM highway then functions as shown below. (FS_X and FS_R may be asynchronous.)



Direct Control Mode

The direct mode of operation will be selected when the CLK_C pin is strapped to the +5 volt supply (V_{CC}). In this mode, the D_C pin is an active low chip select. In other words, when D_C is low, the device transmits and receives in the timeslots which follow the appropriate framing pulses. With D_C high the device is in the powe. down state. Even though CLK_C characteristics are simpler for the 2911A it will operate properly when plugged into a 2911 board.

Deactivation of a channel by removal of the appropriate framing pulse (FS_X or FS_R) is generally not permitted.

Specifically, framing pulses must be applied for a minimum of two frames after a change in state of D_C in order for the D_C change to be internally sensed. In particular, when entering standby in the direct mode, framing pulses must be applied as usual for two frames after D_C is brought high. Thereafter, the framing pulses could, if desired, be removed until such time as the device is to be reactivated by the reapplication of framing pulses with D_C low.

The Codec will enter the direct mode within three frame times (375 μsec) as measured from the time the device power supplies settle to within the specified limits. This assumes that CLK_C is tied to V_{CC} and that all clocks are available at the time the supplies have settled.

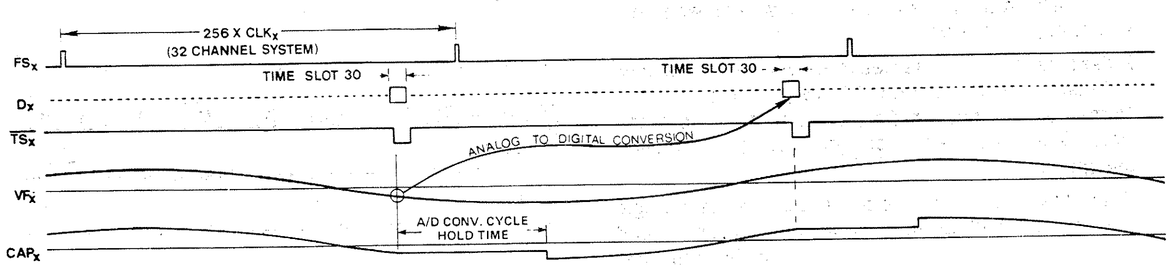
General Control Requirements

All bit and frame clocks should be applied whenever the device is active. In particular, an unused channel cannot be deactivated by removal of its associated frame or bit clock while the other channel of the same device remains active.

A single channel cannot be deactivated except by physical disconnection of the data lead (D_X or D_R) from the system data bus. A device (both transmit and receive channels) may be deactivated in either control mode by powering down the device. Both channels are always powered down together.

Encoding

The VF signal to be encoded is input on the VF_X lead. An internal switch samples the signal and the hold function is performed by the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads. The sampling and conversion is synchronized with the transmit timeslot. The PCM word is then output on the D_X lead at the proper timeslot occurrence of the following frame. The A/D converter saturates at approximately ±2.2 volts RMS (±3.1 volts peak).



Decoding

The PCM word is fetched by the D_R lead from the PCM highway at the proper timeslot occurrence. The decoded value is held on an internal sample and hold capacitor.

The buffered non-return to zero output signal on the VF_R lead has a dynamic range of ±2.2 volts RMS (±3.1 volts peak).

Standby Mode — Power Down

To minimize power consumption and heat dissipation a standby mode is provided where all Codec functions are disabled except for D_C and CLK_C leads. These allow the Codec to be reactivated. In the microcomputer mode the Codec is placed into standby by loading a control word (D_C) with a "1" in bits 1 and 2 locations. In the direct mode when D_C is brought high, the all "1's" control word is internally transferred to the control register, invoking the standby condition.

While in the standby mode, the D_X output is actively held in a high impedance state to guarantee that the PCM bus will not be driven.

The power consumption in the standby mode is typically 33 mW.

Power-On Clear

Whether the device is used in the direct or microcomputer mode, an internal reset (power-on clear) is generated, forcing the device into the power down state, when power is supplied by any of the following methods. (1) Device power supplies are turned on in a system power-up situation where either V_{CC} or V_{DD} is applied last. (2) A large supply transient causes either of the two positive supplies to drop to approximately 2 volts. (3) A board containing Codecs is plugged into a "hot" system where V_{CC} or V_{DD} is the last contact made. It may be necessary to trim back the edge connector pins or fingers on V_{CC} or V_{DD} relative to the other supply to guarantee that the power-on clear will operate properly when a board is plugged into a "hot" system. Furthermore, the Codec will inhibit activity on $\overline{TS}_X$ and D_X during the application of power supplies.

The device is also tolerant of transients in the negative supply (V_{BB}) so long as V_{BB} remains more negative than −3.5 volts. V_{BB} transients which exceed this level should be detected and followed by a system reinitialization.

Precision Voltage Reference for the D/A Converter

The voltage reference is generated on the chip and is calibrated during the manufacturing process. The technique uses the difference in sub-surface charge density between two suitably implanted MOS devices to derive a temperature stable and bias stable reference voltage.

A gain setting op amp, programmed during manufacturing, "trims" the reference voltage source to the final precision voltage reference value provided to the D/A converter. The precision voltage reference determines the initial gain and dynamic range characteristics described in the A.C. Transmission Specification section.

CONVERSION LAW

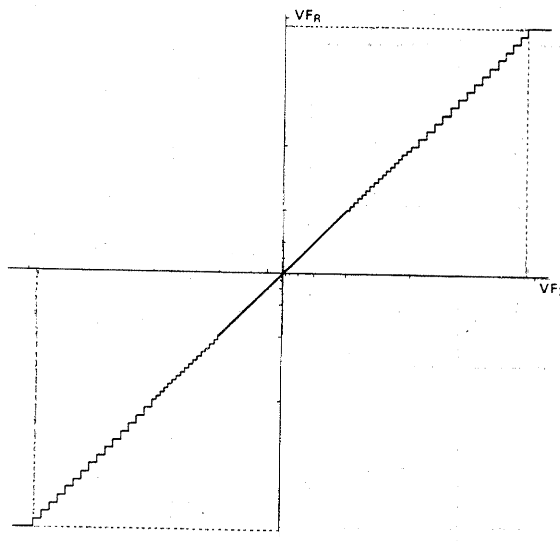
The conversion law is commonly referred to as the A Law.

The Codec provides a piecewise linear approximation of the logarithmic law through 13 segments. Each segment is made of 16 steps with the exception of the first segment, which has 32 steps. In adjacent segments the step sizes are in a ratio of two to one. Within each segment, the step size is constant.

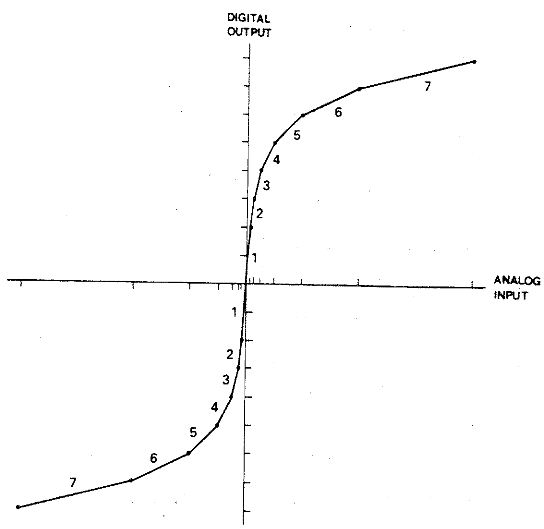
The output levels are midway between the corresponding decision levels. The output levels y_n are related to the input levels x_n by the expression:

$$y_n = \frac{x_{n-1} + x_n}{2}, \quad 0 < n \leqslant 128$$

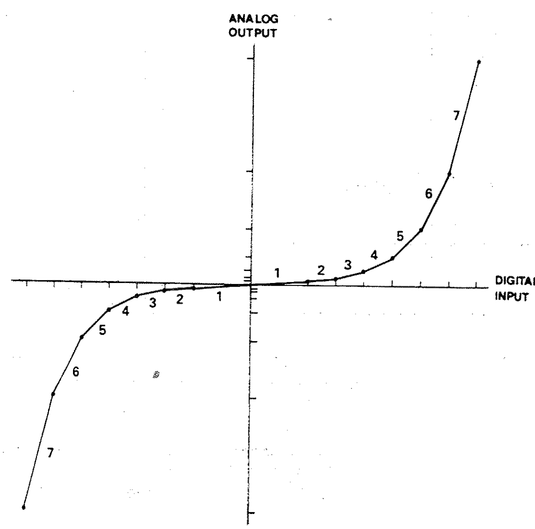
CODEC TRANSFER CHARACTERISTIC



CODER TRANSFER CHARACTERISTIC
(A/D CONVERSION)



DECODER TRANSFER CHARACTERISTIC
(D/A CONVERSION)



Theoretical A-Law — Positive Input Values (for Negative Input Values, Invert Bit 1)

1	2	3	4	5	6	7	8
Segment Number	No. of Steps × Step Size	Value at Segment End Points	Decision Value Number n	Decision Value x_n[1]	PCM Word[4] Bit Number 1 2 3 4 5 6 7 8	Normalized Value at Decoder Output y_n[5]	Decoder Output Value Number
		4096[3]	(128)	(4096)			
					1 1 1 1 1 1 1 1	4032	128
			127	3968			
7	16 × 128				(see Note 2)		
			113	2176			
					1 1 1 1 0 0 0 0	2112	113
		2048	112	2048			
6	16 × 64				(see Note 2)		
			97	1088			
					1 1 1 0 0 0 0 0	1056	97
		1024	96	1024			
5	16 × 32				(see Note 2)		
			81	544			
					1 1 0 1 0 0 0 0	528	81
		512	80	512			
4	16 × 16				(see Note 2)		
			65	272			
					1 1 0 0 0 0 0 0	264	65
		256	64	256			
3	16 × 8				(see Note 2)		
			49	136			
					1 0 1 1 0 0 0 0	132	49
		128	48	128			
2	16 × 4				(see Note 2)		
			33	68			
					1 0 1 0 0 0 0 0	66	33
		64	32	64			
1	32 × 2				(see Note 2)		
			1	2			
					1 0 0 0 0 0 0 0	1	1
			0	0			

Notes:

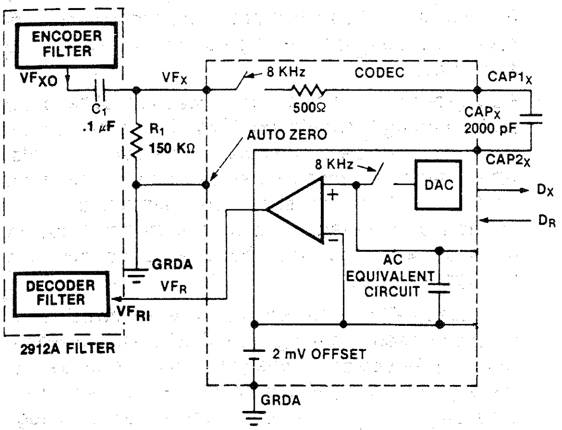
1. 4096 normalized value units correspond to the value of the on-chip voltage reference.
2. The PCM word corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (128 + n) expressed as a binary number.
3. X_{128} is a virtual decision value.
4. The PCM word on the highways is the same as the one shown in column 6, with the even order bits inverted. The 2911A provides for the inversion of the even order bits on both the send and receive sections.
5. The voltage output on the VF_R lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15 mV.

APPLICATIONS

Holding Capacitor

For an 8KHz sampling system the transmit holding capacitor CAP_X should be 2000 pF ± 20%.

Circuit Interface — Without External Auto Zero



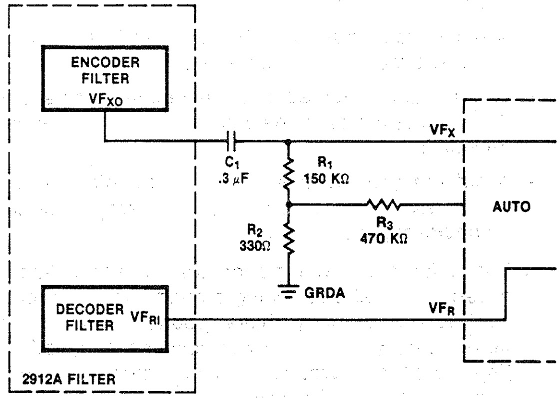
Filters Interface

The filters may be interfaced as shown in the circuit interface diagrams. Note that the output pulse stream is of the non-return-to-zero type and hence requires the (sin x)/x correction provided by the 2912A filter.

D_X Buffering

For higher drive capability or increased system reliability it may be desirable that the D_X output of a group of Codecs be buffered from the system PCM bus with an external three-state or open collector buffers. A buffer can be enabled with the appropriate Codec generated $\overline{TS_X}$ signal or signals. $\overline{TS_X}$ signal may also be used to activate external zero code suppression logic, since the occurrence of an active state of any $\overline{TS_X}$ implies the existence of PCM voice bits (as opposed to transparent data bits) on the bus.

Circuit Interface — With External Auto Zero



Auto Zero

The 2911A contains a transparent on-chip auto zero plus a device pin for implementing a sign-bit driven external auto zero feedback loop. The on-chip auto zero reduces the input offset voltage of the encoder (VF_X) to less than 3 mV. For most telephony applications, this input offset is perfectly acceptable, since it insures the encoder is biased in the lower 25% of the first segment.

Where lower input offset is required the external auto zero loop may be used to bias the encoder exactly at the zero crossing point. The consequence of the external auto zero loop, aside from extra components, is the addition of the dithering auto-zero signal to the input signal, resulting in slightly higher idle channel noise (approximately 2 dB) than when the external loop is not used. Consequently, where the application permits, it is recommended that the external auto zero loop not be used.

The circuit interface without external auto zero shows a possible connection between VF_X and AUTO leads with the recommended values of $C_1 = 0.1\mu F$ and $R_1 = 150 K\Omega$.

The circuit interface with external auto zero drawing shows a possible connection between VF_X and AUTO leads with the recommended values of $C_1 = 0.3\mu F$, $R_1 = 150 K\Omega$, $R_2 = 330\Omega$, and $R_3 = 470 K\Omega$.

Grounding, Decoupling, and Layout Recommendations

The most important steps in designing a low noise line card are to insure that the layout of the circuit components and traces results in a minimum of cross coupling between analog and digital signals, and to provide well bypassed and clean power supplies, solid ground planes, and minimal lead lengths between components.

1. All power source leads should be bypassed to ground on each printed circuit board (PCB), on which codecs are provided. At least one electrolytic bypass capacitor (at least 10μF) per board is recommended at the point where all power traces from the codecs and filters join prior to interfacing with the edge connector pins assigned to the power leads.
2. When using two-sided PCBs, use both corresponding pins on opposite sides of the board for the same power lead. Strap them together both on the PCB and on the back of the edge connector.
3. Lay out the traces on codec- and filter-equipped boards such that analog signal and capacitor leads from the digital clock and data leads are separated as widely as possible.
4. Connect the codec sample and hold capacitor with the shortest leads possible. Mount them as close to the device pins as can be achieved. Shield the capacitor traces with analog ground.
5. Do not lay out any board traces (especially digital) that pass between or near the leads of the sample and hold capacitor(s) since they are in high impedance circuits which are sensitive to noise coupling.
6. Keep analog voice circuit leads paired on their

layouts so that no intervening circuit leads are permitted to run parallel to them and/or between them.

7. Arrange the layout for each duplicated line, trunk or channel circuit in identical form.

8. Line circuits mounted extremely close to adjacent line circuits increase the possibility of interchannel crosstalk.

9. Avoid assignment of edge connector pins to any analog signal adjacent to any lead carrying digital (periodic) signals or power.

10. The optimum grounding configuration is to maintain separate digital and analog grounds on the circuit boards, and to carry these grounds back to the power supply with a low impedance connection. This keeps the grounds separate over the entire system except at the power supply.

11. The voltage difference between ground leads GRDA and GRDD (analog and digital ground) should not exceed two volts. One method of preventing any substantial voltage difference between leads GRDA and GRDD is to connect two diodes back to back in opposite directions across these two ground leads on each board. An additional or alternate method of suppressing ground lead noise is to bridge a RF choke of about 1 to 2μH or greater, as space allows, between leads GRDA and GRDD on each board.

12. Codec-filter pairs should be aligned so that pins 9 through 16 of the filter face pins 1 through 12 of the codec. This minimizes the distance for analog connections between devices and with no crossing analog lines.

13. No digital or high voltage level (such as ringing supply) lines should run under or in parallel with these analog VF connections. If the analog lines are on the top (component side) of the PC board, then GRDD, GRDA, or power supply leads should be directly under them, on the bottom to prevent analog/digital coupling.

14. Both the codec and filter devices should be shielded from traces on the bottom of the PCB by using ground or power supply leads on the top side directly under the device (like a ground plane).

15. Two +5 volt power supply leads (V_{CC}) should be used on each PCM, one to the filters, the other to the codecs. These leads should be separately decoupled at the PCB where they then join to a single 5 volt supply at the backplane connector. Decoupling can be accomplished with either a series resistor/parallel capacitor (RC lowpass) or a series RF choke and parallel capacitor for each 5 volt lead. The capacitor should be at least 10μF in parallel with a 0.1μF ceramic. This filters both high and low frequencies and accommodates large current spikes due to switching.

16. Both grounds and power supply leads must have low resistance and inductance. This should be accomplished by using a ground plane whenever possible. When narrower traces must be used, a minimum width of 4 millimeters should be maintained. Either multiple or extra large plated through holes should be used when passing the ground connections through the PCB.

17. The 2912A PCM filter should have all power supplies bypassed to analog ground (GRDA). The 2911A Codec +5V power supplies should be bypassed to the digital ground (GRDD). This is appropriate when separate +5V power supply leads are used as suggested in item 15. The −5V and +12V supplies should be bypassed to analog ground (GRDA). Bypass capacitors at each device should be high frequency capacitors of approximately 0.1 to 1.0 μF value. Their lead lengths should be minimized by routing the capacitor leads to the appropriate ground plane under the device (either GRDA or GRDD).

18. Relay operation, ring voltage application, interruptions, and loop current surges can produce enormous transients. Leads carrying such signals must be routed well away from both analog and digital circuits on the line card and in backplanes. Lead pairs carrying current surges should be routed closely together to minimize possible inductive coupling. The microcomputer clock lead is particularly vulnerable, and should be buffered. Care should also be used in the backplane layout to prevent pick-up surges. Any other latching components (relay buffers, etc.) should also be protected from surges.

Absolute Maximum Ratings*

Temperature Under Bias .... −10°C to +80°C
Storage Temperature .... −65°C to +150°C
All Input or Output Voltages with Respect to V_{BB} .... −0.3V to +20V
V_{CC}, V_{DD}, GRDA, and GRDA with Respect to V_{BB} .... −0.3V to +20V
Power Dissipation 1.35W

***Comment:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. and Operating Characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Symbol	Parameter	Limits Min	Typ[1]	Max	Unit	Test Conditions
DIGITAL INTERFACE						
I_{IL}	Low Level Input Current			10	μA	$V_{IN} < V_{IL}$
I_{IH}	High Level Input Current			10	μA	$V_{IN} > V_{IH}$
V_{IL}	Input Low Voltage			0.6	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.4	V	D_X, $I_{OL} = 4.0mA$ $\overline{TS_X}$, $I_{OL} = 3.2mA$, open drain PDN, $I_{OL} = 1.6mA$, open drain
V_{OH}	Output High Voltage	2.4			V	D_X, $I_{OH} = 15mA$
ANALOG INTERFACE						
Z_{AI}	Input Impedance when Sampling, VF_X	125	300	500	Ω	In series with CAP_X to GRDA, $-3.1V < V_{IN} < 3.1V$
Z_{AO}	Small Signal Output Impedance, VF_R	100	180	300	Ω	$-3.1V < V_{OUT} < 3.1V$
V_{OR}	Output Offset Voltage at VF_R	−50		50	mV	Minimum code to D_R
V_{IX}	Input Offset Voltage at VF_X	−5		5	mV	Minimum positive code produced at D_X
V_{OL}	Output Low Voltage, Auto Zero		V_{BB}	$(V_{BB} + 2)$	V	400KΩ to GRDA
V_{OH}	Output High Voltage, Auto Zero	$(V_{CC} - 2)$	V_{CC}		V	400KΩ to GRDA
POWER DISSIPATION						
I_{DDO}	Standby Current		0.7	1.1	mA	
I_{CCO}	Standby Current		4.0	7.0	mA	
I_{BBO}	Standby Current		1.0	2.5	mA	clock frequency = 2.048MHz
I_{DDI}	Operating Current		11	16	mA	
I_{CCI}	Operating Current		13	21	mA	
I_{BBI}	Operating Current		4.0	6.0	mA	

Notes:
1. Typical values are for $T_A = 25°C$ and nominal power supply values.

A.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ[1]	Limits Max	Unit	Test Conditions
TRANSMISSION (any two Codecs, end-to-end, unless otherwise specified)						
S/D	Signal to Total Distortion Ratio. CCITT G.712 Method 1	TBD	TBD		dB	signal level −3dBm0 to −6dBm0
		TBD	TBD		dB	Signal level to −27dBm0
		TBD	TBD		dB	Signal level to −34dBm0
		TBD	TBD		dB	Signal level to −40dBm0
		TBD	TBD		dB	Signal level to −55 dBm0
S/D	Signal to Total Distortion Ratio. See Figure 2. CCITT G.712 Method 2	35			dB	Signal level 0dBm0 to −30dBm0
		29			dB	Signal level to −40dBm0
		24			dB	Signal level to −45dBm0
S/D	Signal to Total Distortion Ratio. CCITT G.712 Method 2 (Half Channel)	TBD	TBD		dB	Signal level 0dBm0 to −30dBm0
		TBD	TBD		dB	Signal level to −40dBm0
		TBD	TBD		dB	Signal level to −45dBm0
ΔG	Gain Tracking Deviation from Gain at 0dBm0. CCITT G.712 Method 1	TBD	TBD		dB	Signal level +3dBm0 to −10dBm0
		TBD	TBD		dB	Signal level to −55dBm0
		TBD	TBD		dB	Signal level to −60dBm0
ΔG	Gain Tracking Deviation from Gain at 0dBm0. See Figure 1. CCITT G.712 Method 2	−0.4		0.4	dB	Signal level +3dBm0 to −40dBm0
		−0.8		0.8	dB	Signal level to −50dBm0
		−2.4		2.4	dB	Signal level to −55dBm0
ΔG	Gain Tracking Deviation from Gain at 0 dBm0. CCITT G.712 Method 2. (Half Channel)	TBD	TBD		dB	Signal level +3dBm0 to −40dBm0
		TBD	TBD		dB	Signal level to −50 dBm0
		TBD	TBD		dB	Signal level to −55dBm0
N_{IC}	Idle Channel Noise		−85	−78	dBm0p	See Note 2
HD	Harmonic Distortion (2nd or 3rd)		−48	−44	dB	$VF_X = 1.02$ KHz, 0dBm0; measured at decoder output VF_R
	Intermodulation Distortion					See Note 3
IMD_1	G.712 (8.1)			−45	dB	
IMD_2	G.712 (8.2)			−50	dB	

Notes:
1. Typical values are for $T_A = 25°C$ and nominal power supply values.
2. If the external auto zero is used N_{IC} has a typical value of −76dBm0.
3. According to the two tone method. CCITT G.712 recommendation.

A.C. Characteristics (continued)

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ[1]	Max		
GAIN AND DYNAMIC RANGE						
DmW	Digital Milliwatt Response	5.56	5.66	5.76	dBm	23°C, nominal supplies[4]
DmW_T	DmW_O Variation with Temperature		−0.001	−0.002	dB/°C	Relative to 23°C[4]
DmW_S	DmW_O Variation with Supplies			±0.07	dB	Supplies ±5%[4]
A_{IR}	Input Dynamic Range	2.17	2.20	2.23	V_{RMS}	Using D.C. and A.C. tests[5]
A_{IRT}	Input Dynamic Range vs Temperature			−0.5	mV_{RMS}/°C	Relative to 23°C
A_{IRS}	Input Dynamic Range vs Supplies			±18	mV_{RMS}	Supplies ±5%
A_{OR}	Output Dynamic Range, VF_R	2.13	2.16	2.19	V_{RMS}	23°C, nominal supplies
A_{ORT}	A_{OR} Variation with Temperature			−0.5	mV_{RMS}/°C	Relative to 23°C
A_{ORS}	A_{OR} Variation with Supplies			±18	mV_{RMS}	Supplies ±5%
SUPPLY REJECTION AND CROSSTALK						
$PSRR_1$	V_{DD} Power Supply Rejection Ratio	50			dB	decoder alone[6]
$PSRR_2$	V_{BB} Power Supply Rejection Ratio	35			dB	decoder alone[6]
$PSRR_3$	V_{CC} Power Supply Rejection Ratio	50			dB	decoder alone[6]
$PSRR_4$	V_{DD} Power Supply Rejection Ratio	50			dB	encoder alone[7]
$PSRR_5$	V_{BB} Power Supply Rejection Ratio	45			dB	encoder alone[7]
$PSRR_6$	V_{CC} Power Supply Rejection Ratio	50			dB	encoder alone[7]
CT_R	Crosstalk Isolation, Receive Side	75	80		dB	See Note 8
CT_T	Crosstalk Isolation, Transmit Side	75	80		dB	See Note 9
CAPX	Input Sample and Hold Capacitor	1600	2000	2400	pF	

Notes:

4. D_R of Device Under Test (D.U.T.) driven with repetitive digital word sequence specified in CCITT recommendation G.711. Measurement made at VFR output.
5. With the D.C. method the positive and negative clipping levels are measured and A_{IR} is calculated. With the A.C. method a sinusoidal input signal to VF_X is used where A_{IR} is measured directly.
6. D.U.T. decoder; impose 200 mV_{P-P}, 1.02 KHz on appropriate supply; measurement made at decoder output; decoder in idle channel conditions.
7. D.U.T. encoder, impose 200 mV_{P-P}, 1.02 KHz on appropriate supply; measurement made at encoder output; encoder in idle channel conditions.
8. VF_X of D.U.T. encoder = 1.02 KHz, 0 dBm0. Decoder under quiet channel conditions; measurement made at decoder output.
9. VF_X = 0 Vrms. Decoder = 1.02 KHz, 0 dBm0. Encoder under quiet channel conditons; measurement made at encoder output.

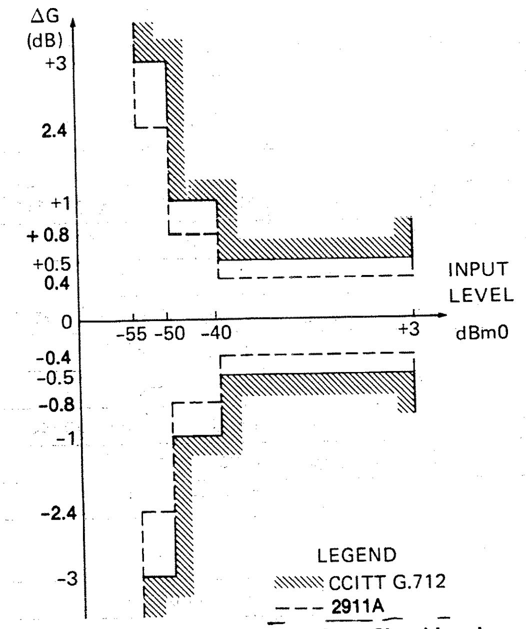


Figure 1. Gain Variation (ΔG) vs. Signal Level Reference Level 0 dBm0, End-to-End

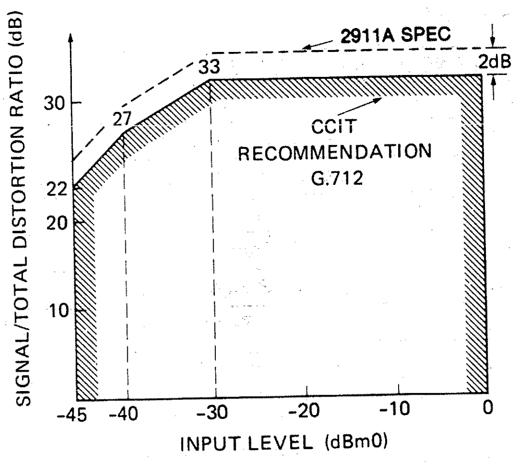
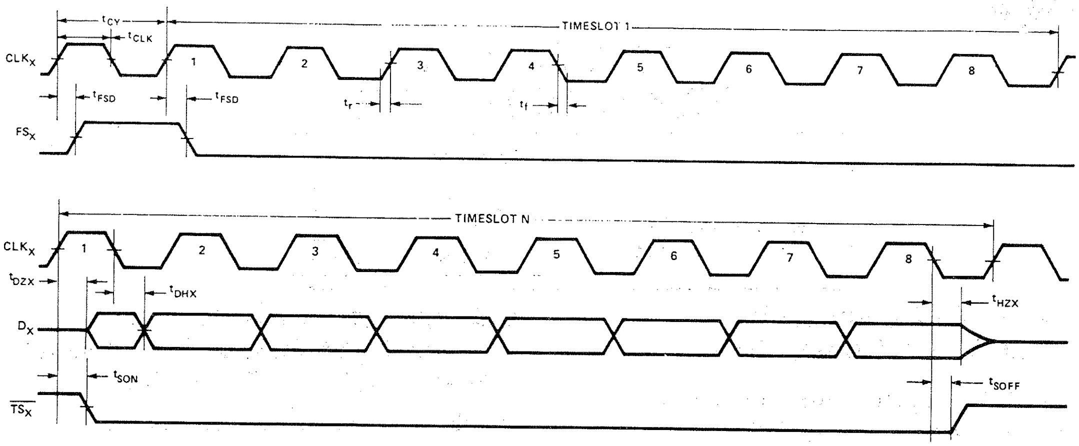


Figure 2. Signal/Total Distortion Ratio, End-to-End

A.C. Characteristics — Timing Specification and Waveforms[1]

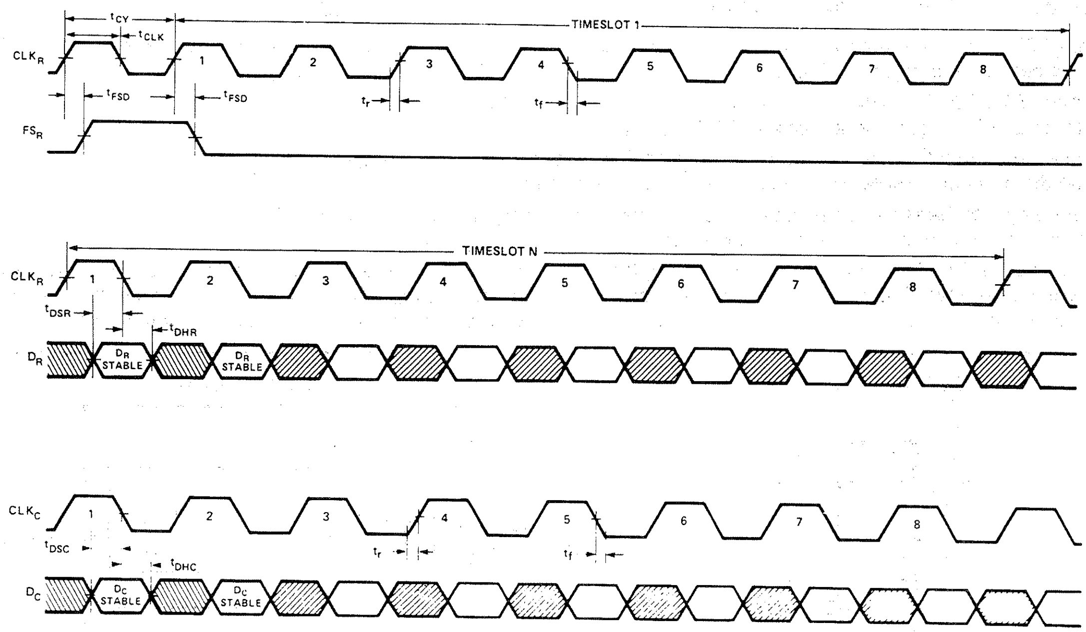
$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Symbol	Parameter	Limits		Units	Comments
		Min	Max		
CLOCK SECTION					
t_{CY}	Clock Period	485		ns	CLK_X, CLK_R (2.048 MHz systems), CLK_C
t_r, t_f	Clock Rise and Fall Time	0	30	ns	CLK_X, CLK_R, CLK_C
t_{CLK}	Clock Pulse Width	215		ns	CLK_X, CLK_R, CLK_C
t_{CDC}	Clock Duty Cycle ($t_{CLK} \div t_{CY}$)	45	55	%	CLK_X, CLK_R
TRANSMIT SECTION					
t_{VFX}	Analog Input Conversion	20		timeslot	from leading edge of transmit timeslot[2]
t_{DZX}	Data Enabled on TS Entry	50	180	ns	$0 < C_{LOAD} < 100\,pF$
t_{DHX}	Data Hold Time	80	230	ns	$0 < C_{LOAD} < 100\,pF$
t_{HZX}	Data Float on TS Exit	75	245	ns	$C_{LOAD} = 0$
t_{SON}	Timeslot X to Enable	30	185	ns	$0 < C_{LOAD} < 100\,pF$
t_{SOFF}	Timeslot X to Disable	70	225	ns	$C_{LOAD} = 0$
t_{FSD}	Frame Sync Delay	15	150	ns	
RECEIVE AND CONTROL SECTIONS					
t_{VFR}	Analog Output Update	7 1/16	7 1/16	timeslot	from leading edge of the channel timeslot
t_{DSR}	Receive Data Setup	20		ns	
t_{DHR}	Receive Data Hold	60		ns	
t_{FSD}	Frame Sync Delay	15	150	ns	
t_{DSC}	Control Data Setup	100		ns	Microcomputer mode only
t_{DHC}	Control Data Hold	100		ns	Microcomputer mode only



Notes:

1. All timing parameters referenced to 1.5V, except t_{HZX} and t_{SOFF}, which reference a high impedance state.
2. The 20 timeslot minimum insures that the complete A/D conversion will take place under any combination of receive interrupt or asynchronous operation of the Codec. Consult an Intel applications specialist or Intel Corporation for applications information which would allow operation with less than 20 timeslots.



Notes:

1. All timing parameters referenced to 1.5V, except t_{HZX} and t_{SOFF} which reference a high impedance state.