General Description

RT0032 is a 32-stage charge-transfer device which permits the storage of analog signals with recovery of the signals at multiple separate outputs at successive delay times later. The taps on each stage are brought to the outside through buffer amplifiers. Each buffer amplifier output appears as a source follower, thus permitting variable loading of the taps in order to create various tap-weight functions. The taps are spaced one sample time apart along the delay. An additional special feed-forward output tap is provided so that multiple devices may be cascaded without causing discontinuity in the spacing of the taps from one device to the next. With this arrangement, timing integrity is maintained. The ability to cascade devices permits the user to build processors (such as transversal filters) with more than 32 taps.

The Reticon RT0032 is a tapped analog delay line fabricated with the most advanced n-channel silicon-gate integrated-circuit technology. It consists of a charge-transfer device with 32 taps equally spaced one sample-time apart along the device. It is designed specifically for use in the realization of transversal filters, but it likewise is applicable to recursive or other filter types. Typical applications include: lowpass filters, bandpass filters, matched filters, phase equalizers, phase shifters, tone generators, function generators, correlators, and simple tapped delays.

Key Features

- **Monolithic construction**
- **Full wave output from each tap**
- **32 equally spaced taps, with separate feed-forward tap**
- **Buffered outputs from each tap**
- **Tap delay linearly variable with clock period**
- **Sampling rates to 5 MHz**
- **40 db passband-to-stopband ratio (as a filter)**
- **60 db dynamic range**
- **Simple I/O and clock circuit**
- **Low power dissipation**
- **40-pin dual-in-line package**

Device Operation

The equivalent circuit is shown in Figure 1. Samples are set up on the initial storage node during the time period when the $\emptyset_1$ clock waveform is at its high (positive) level. When $\emptyset_1$ drops, the sample value is frozen and the simultaneous rise of $\emptyset_2$ permits exchange of charge with the tap-1 node; similarly for other nodes. The sample values thus first appear at the various tap outputs when $\emptyset_2$ rises. When $\emptyset_2$ falls and $\emptyset_1$ rises, the charge state is transferred to the second node for each tap. The paralleling of the buffer outputs thus maintains the output value at the tap for both halves of the clock period. The resulting output is a full-wave (or full period) output. Further, there is one sample time delay between the samples as they appear at successive output taps. The last node supplies a feed-forward tap at the proper time to provide the set-up signal for another, series-connected RT0032, so that multiple-section processors with more than 32 taps can be implemented. Clocking of the second device must be synchronous with the first, i.e., $\emptyset_{1A} = \emptyset_{1B}$.

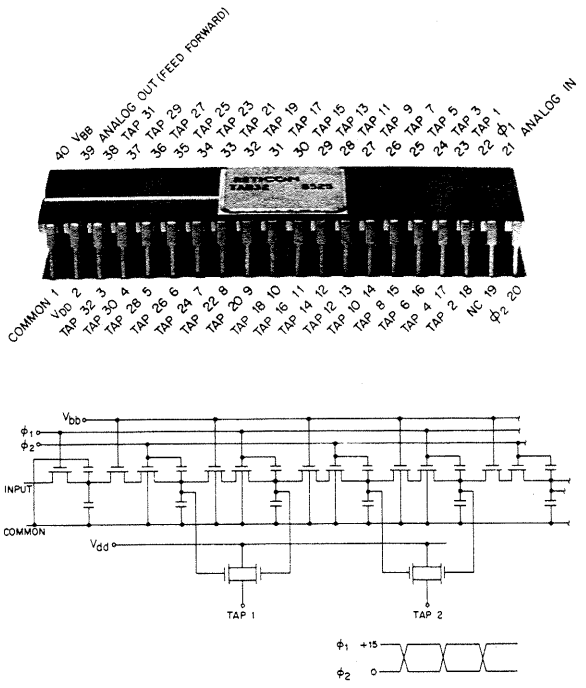

Figure 1. A tapped analog delay line made using metal-oxide-silicon integrated circuit technology.

The device is capable of sampling rates from below 1KHz to more than 5 MHz. This capability permits the translation of a given filter characteristic over a range of more than three orders of magnitude in frequency simply by varying the clock rate. A two-phase complementary square-wave clock with amplitude in the range of 12 to 15 volts is required to drive the device. The clock phases are positive square waves, as shown in the inset of Figure 1 and in more detail in Figure 2. The clocks drive the nodes positive, thus providing a positive output with reference to ground at each tap. The output from each tap is a full-wave or boxcar output, as discussed above; no additional filtering is necessary before summing with the desired weights. The summing amplifiers can combine the summing and filtering functions.

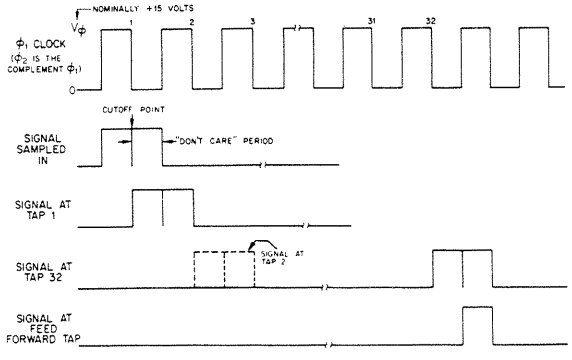

Figure 2. Relative timing diagram.

345 POTRERO AVENUE SUNNYVALE, CALIFORNIA 94086-4197 (408) 738-4266 TWX: 910-339-9343

Functional Performance

The RT0032 functions as a discrete-time processor. Time is quantized, but signal amplitudes retain the analog values associated with the discrete-time values corresponding to the falling edges of $\emptyset_1$ (the sample times). Behavior is that of a discrete-time or sampled-data system. The specifications and performance data thus must be interpreted in the light of such a system. An indication of the performance is given in Figures 3 and 4 for the simple equal-tap-weight case.

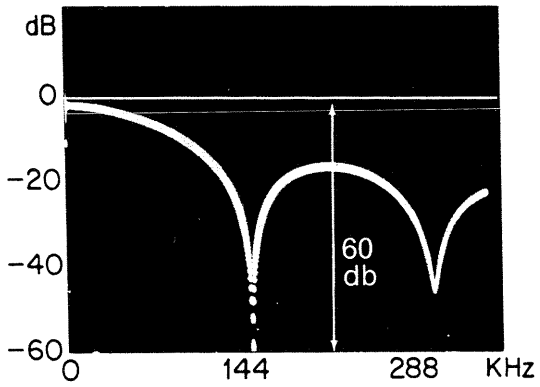

Figure 3. Frequency spectrum for equal-weight FIR filter; 3 MHz clock frequency, 3 Hz resolution bandwidth, 360 KHz scan. (Note the 60-db dynamic range as shown by the null depth.)

1. Example of Performance

The simplest form of a low pass filter has all taps weighted equally and summed. For this equal-weight transversal filter, the frequency response is as shown in Figure 3 above. The impulse response, which bears a unique relationship to the frequency response, is shown in Figure 4. Filter design may be based on a desired frequency response, but generally proceeds by first finding the impulse response corresponding to the frequency response.

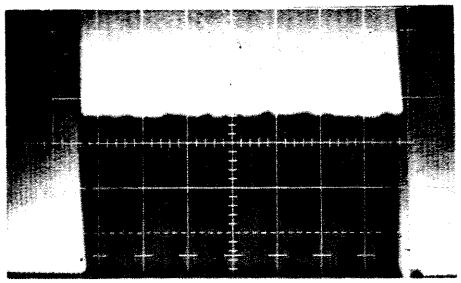

Figure 4. Oscillogram of equal-weight impulse response.

For the case of Figure 4, a single (unit-weight) sample is provided as input. This sample then appears once at each tap output, then moves to the next, and finally out of the system. Thus, the summed tap outputs is a string of 32 successive unit-amplitude segments as in Figure 4. The frequency response for this case is ideally $\sin(32\ \pi\ f_S/f_C)/\sin(\ \pi\ f_S/f_C)$, where f_S is the signal frequency and f_C the sample frequency. The spectrum of Figure 3 shows this pattern with a 60-db null depth. The resolution bandwidth was 3 Hz and the frequency scan 0 to 360 KHz. A careful plot of data derived from Figure 3 is indistinguishable from the theoretical response.

It is obvious that the equal-tap-weight described in Example 1 gives a form of low pass filtering. However, the filter is far from ideal even with perfect performance. Side lobes are large, and the general stop-band performance is poor. A basic improvement is described in Example 2.

2. Example of tap-weight tailoring for improved performance

The difficulty with the filter of Example 1 lies in the very simplicity of the tap weights. As illustration, suppose we postulate an "ideal" rectangular passband. Such a passband requires an impulse response approximating a sin x/x form, extending over all time. Since, however, such an "ideal" response is impractical to achieve, we modify the sin x/x function by multiplying tap weight values by a Hamming window[1] weighting function. This gives major weight to central taps and diminishing weight to outer taps, decreasing to zero where we run out of taps because of finite limitations on the possible number. Such a weighting, for 16 taps between zero crossings of the weighted sin x/x function, is shown in Figure 5 as a calculated oscilloscope overlay. An actual measured impulse response corresponding to this weighting is shown in Figure 6, and the frequency response, measured with a spectrum analyzer of 1 KHz resolution bandwidth, is shown in Figure 7. Further details of the measurements and design procedure may be found in Refs. 1 and 2. For Figures 6 and 7, tap weights were initially selected to 1%, then the major taps slightly altered by simply adjusting the tap weights until the actual output best approximates the desired pattern overlaid on the face of the oscilloscope (see Figure 5).

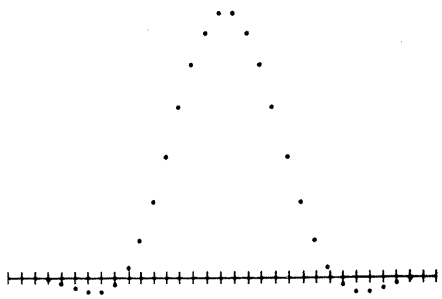

Figure 5. Oscilloscope overlay for Hamming-windowed sin x/x impulse response, 16 taps between zero crossings.

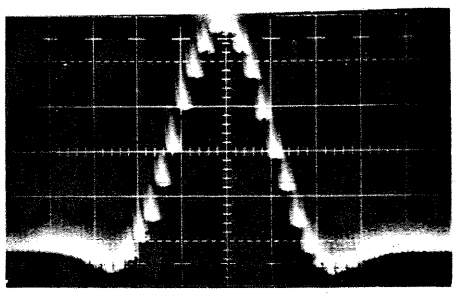

Figure 6. Actual impulse response matching Figure 5.

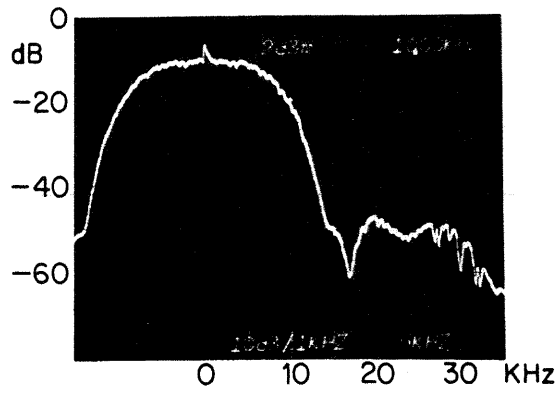

Figure 7. Frequency spectrum, wide band, corresponding to impulse response of Figure 6.

Dynamic Range

The usable dynamic range normally exceeds 60 db, as shown in Figures 3 and 8. The data were taken on a spectrum analyzer, which provided the required filtering against clock noise, while retaining any spurious or harmonic responses, as well as showing the noise floor. In any normal application, adequate input and output filtering are an integral part of the design. The input filter is required to prevent aliasing responses, the output filter to separate base-band components from the clock-frequency components (and harmonics). The latter also serves to smooth the full-period boxcar variation of the individual or summed outputs so as to recover the base-band components. The dynamic-range measurements of Figure 8 are applicable to the low-pass filters of the examples.

Linearity, Distortion, and Noise

These attributes of the device give supplemental measures of its performance. For small signals, the relationship between input and output is highly linear. As the signal amplitude increases, slight departure from linearity occurs. Ultimately, an overload limit is reached where a rapid onset of clipping distortion accompanies any further signal increase. The rapid rise of distortion with excessively high signal level is indicated by the data of Figure 8. The linearity and distortion data are obtained from single-tap measurements.

Noise is of two general types: (a) clock-related noise which can largely be eliminated by appropriate output filtering, and (b) random noise, which arises from statistical charge variations, resistance in transfer paths, and miscellaneous other sources. Without filtering, the clock noise is dominant, but this noise is largely removable by appropriate output filters. The residue after filtering, particularly that within the desired signal band, sets the lower signal limit. On a broadband oscilloscope presentation the tangential noise is more than 40 db below a 4V p-p reference signal. In a 3 KHz filter band, the noise is more than 60 db below the reference signal, as indicated in Figure 8. This figure shows various measurements taken on a single-tap basis; multiple-tap performance is illustrated by Figure 3.

As with all solid-state devices, elevated temperature increases background current and hence increases noise. It also modifies slightly the desired bias point, particularly at low clock frequencies where delay is maximum. But because there are only 64 charge transfers per device, the effects are minimal. Performance at very low clocking frequencies is most affected by elevated temperature because of the increased discharging effect of the leakage (background) current. Increasing the temperature increases the leakage and thus increases the minimum sampling frequency by a factor of two for every 7°C increase above normal room temperature.

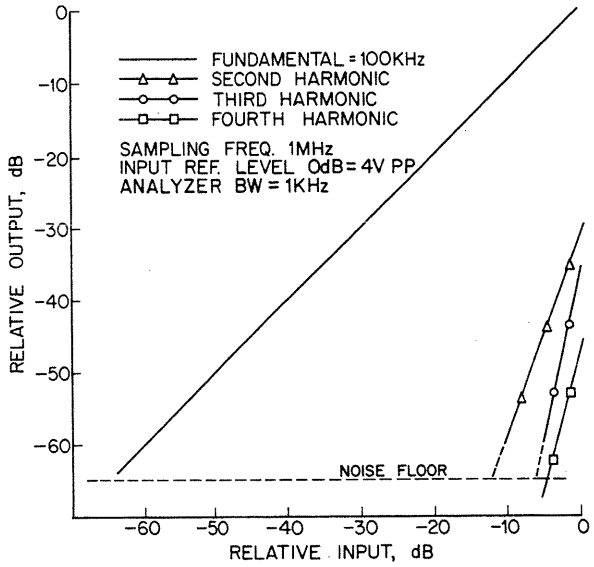

Figure 8. RT0032 single-tap performance.

Frequency Response

It should be remembered that the RT0032 is a sampled-data system. Input signals may be successfully sampled at rates up to 5 MHz. Low-frequency signals are sampled many times per cycle and reproduced at the output without loss. High frequency signals when sampled and reestablished are subject to a $\sin(\pi f_S/f_C)/(\pi f_S/f_C)$ roll off, characteristic of sampled data systems. The device itself introduces negligible attenuation.

Drive Circuit

A suitable drive circuit is illustrated in Figure 9. The Schottky TTL flip-flop converts the input clock (at $2f_C$) into the desired complementary square-wave clock signals at Q and Q. Rise and fall times are adequately short (less than 20 nsec) and skew is minimal (waveforms cross at the approximate 50% level). The 0026 translator (National or Motorola) converts the amplitude and level to those required by the RT0032 while preserving the integrity of the waveforms.The output bias and signal summing arrangements have evolved to the circuit shown in Figure 9 as the best compromise to conflicting requirements. For equal tap weights, the potentiometers are offset by equal amounts (i.e., resistor values to the + line are all equal, as are the complementary values to the – line; a centered potentiometer gives zero tap weight); for other filter arrangements, the ratio of the resistances determines the tap weight. The ST0032A Evaluation Circuit Card incorporates the test circuit shown in Figure 9.

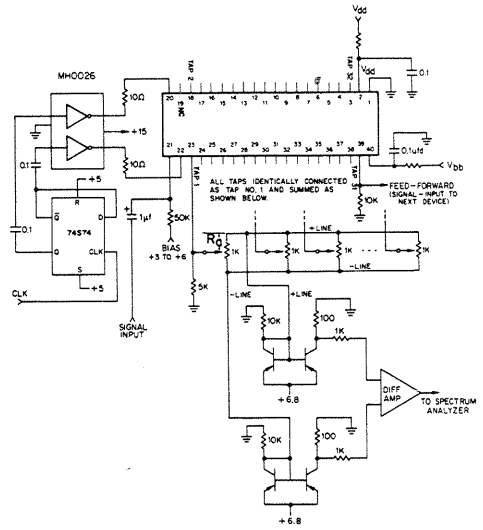

Figure 9. RT0032 test circuit.

To obtain a greater number of taps, devices may be cascaded using synchronous clocks. The feed-forward output of the first device becomes the input to the second device. Figure 9 shows the required arrangements and d-c load on the feed-forward tap – pin 39 – (the latter is needed only when cascading multiple devices). The circuit of Figure 10 permits an adjustment of gain to unity, and the SD210 source follower provides the requisite buffer to give good high-frequency performance when driving a capacitive load. A bipolar transistor in place of the SD210 is less suitable because of its larger effective input capacitance.

In normal operation, V_{dd} operates at the same level as the clock; V_{bb} is preferably adjusted to a slightly lower potential; in the region of zero to one volt *lower* than the maximum voltage of the clock. Since, with the 0026, the maximum clock voltage is approximately one diode drop below V_{dd}, an adjustment of V_{bb} approximately one to one and one-half volts below V_{dd} is typical.

Although the clock drive circuit shown is preferred, a CMOS D-type flip-flop, such as the type 4013 (B version preferred), will directly provide complementary clock waveforms which are adequate for many applications.

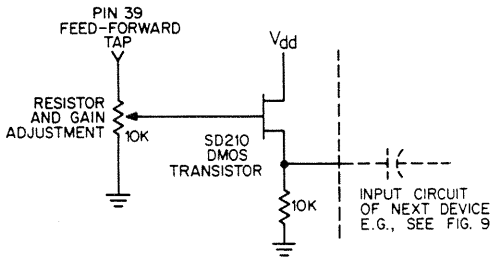

Figure 10. Suggested interface for serial operation. Clocks are synchronous.

Note that there are conflicting requirements in the tap output circuit. For linearity and minimization of tap-to-tap crosstalk, it is desirable that the taps see a relatively low a-c impedance; further, d-c coupling is desirable to avoid coupling difficulties at low scan rates. On the other hand, it is desirable that the d-c current level be much less than would flow into a low-resistance path to ground. Further, individual differences in source-follower thresholds, etc. give rise to a tap-to-tap variation which requires relatively low gain until the differential combination has been accomplished. The circuit of Figure 9 compromises effectively among the above factors. Weighting is adjustable over the range $-1 \leq W \leq +1$ for each tap by adjustment of the ratio of resistances connecting the + line and – line, respectively. Designated as R_a the resistance between the potentiometer slider and the positive bus, where $0 \leq R_a \leq 1000$ ohms. Then R_a = 500 ohms gives the central or zero-weight value, R_a = 0 gives the maximum positive weight, and R_a = 1000 ohms gives the maximum negative weight. The tap weight is then given by $W = (500 - R_a)/500$, or the resistance value by $R_a = 500\ (1-W)$ ohms where W is the tap weight and is $-1 \leq W \leq +1$. Note that resistance values other than 1000 ohms are possible; higher values lead to excessive crosstalk and lower values lead to excessive d-c balance sensitivity.

It is important that an active tap see a low a-c impedance; a potential variation at the tap couples a small charge variation into the next earlier and next later charge packet. In a filter application such crosstalk merely requires slight adjustment of the tap weights, but it is better to avoid the coupling by means of low impedance load. For the same reason, unused taps should either be left floating or, preferably, connected to V_{dd}. They should *not* be loaded or connected to common, both to avoid crosstalk and to avoid dissipation.

ST0032A Evaluation Circuit Card

The ST0032A Evaluation Circuit Card incorporates the basic circuit shown in Figure 9 and is available from RETICON. It provides the required peripheral circuitry including bias, signal buffering, and clock and start waveforms. External interface with timing logic, etc. is at TTL level to assist in function use of the RT0032. The board may be incorporated into systems, if desired, and is particularly useful during evaluation and initial system design. A descriptive data sheet is available for the ST0032A. The board is available in three versions, designated by dash numbers (–01), (–02), and (–03).

The (–01) version is standard and has fixed resistors of 800 ohms and 200 ohms in place of the potentiometers of Figure 9: all weights are of the same polarity.

The (–02) version is the most versatile, with adjustable tap-weight potentiometers as shown in Figure 9.

The (–03) version is supplied without weighting resistors, so that any customer-desired weighting arrangement may be implemented.

References

1. G.P. Weckler: "A Tapped Analog Delay for Sampled Data Signal Processing" (Reticon Application Note No. 105)
2. R.R. Buss and S.C. Tanaka: "Implementation of Discrete-Time Analog Filter and Processing Systems" (Reticon Application Note No. 111)
3. U. Strasilla, G.P. Weckler: "Charge Transfer Devices for Sampled-Data Processing" (Reticon Application Note No. 114)

Specifications (25°C)

Absolute Maximum Rating	Min.	Max.	Units
Voltage on any terminal with respect to common	–0.4	+20	Volts
Storage temperature	–55	+125	° C
Temperature under bias	–55	+85	° C

Drive	Min.	Typical	Max.	Units
Clock frequency	0.001		5*	MHz
Clock amplitude, $V_{\emptyset}$ (Figures 1, 2)	10	15	16	Volts
Clock line capacitance (each)		50		pf
V_{bb} (optimum)		$V_{\emptyset}$–1	$V_{\emptyset}$	Volts
V_{dd}	$V_{\emptyset}$	+15	16	Volts
DC power dissipation**		200	700	mwatts

* Performance degraded above 2 MHz clock rate.

** DC power dissipation is strongly dependent on the number of taps used and on tap load currents. When all 32 taps are used with 10 K ohm loads, typical dissipation is 200 mwatts.

*** Optimum bias is dependent on clock and supply voltages.

WARNING: Damage to the device may result if the input terminal is a.c. coupled. When the power is removed from the device while signal is applied to input terminal, the substrate may become biased in the forward direction causing the input gate protection to "short circuit."

Input/Output	Typical	Max.	Units
Input capacitance @ +4 V Bias	8		pf
Output capacitance of each tap @ +5 V Bias	3		pf
Output transconductance (at +5 V level, 10 K Ω d-c load)	1.1		ma/v
Input Bias***	3		Volts
Input Signal (p-p)		4	Volts
Tap d-c level	+5		Volts
Unused taps	Connect to V_{dd}		
Performance Characteristics			
A. Single-tap response:			
Dynamic range (See Figures 3 and 8)	60		db
Linearity (See Figure 8)			
Harmonic intercepts (See Figure 8)			
B. 32-tap summed response:			
Dynamic range (See Figure 3)	60		db
Input sensitivity, S/N ~ 1	4		mV p-p