

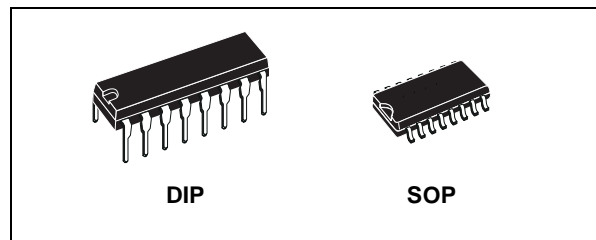


32-STAGE STATIC LEFT/RIGHT SHIFT REGISTER

- FULLY STATIC OPERATION
- SHIFT LEFT/SHIFT RIGHT CAPABILITY
- MULTIPLE PACKAGE CASCADING
- RECIRCULATE CAPABILITY
- LIFO OR FIFO CAPABILITY
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_l = 100\text{nA (MAX) AT } V_{DD} = 18\text{V } T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

DESCRIPTION

HCF40100B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF40100B is a 32-stage shift register containing 32 D-Type master slave flip-flops. The data present at the SHIFT RIGHT INPUT is synchronously transferred into the first register stage with the positive CLOCK edge, provided the LEFT/RIGHT CONTROL is at a low level, the RECIRCULATE CONTROL is at a high level, and the CLOCK INHIBIT is low. If the LEFT/RIGHT control and the RECIRCULATE CONTROL are both at a high level, data at the SHIFT LEFT INPUT is synchronously transferred into the 32nd

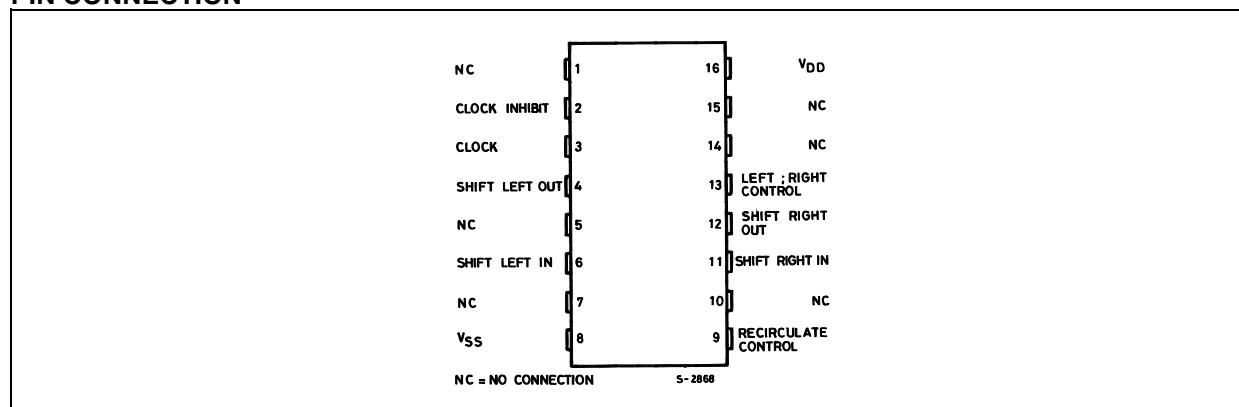


ORDER CODES

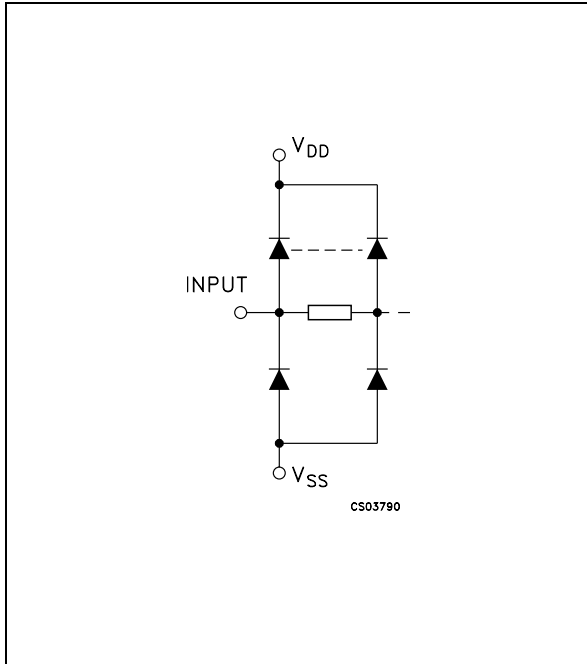
PACKAGE	TUBE	T & R
DIP	HCF40100BEY	
SOP	HCF40100BM1	HCF40100M013TR

register stage with the positive CLOCK transition, provided the CLOCK INHIBIT is low. The state of the LEFT/RIGHT CONTROL, RECIRCULATE CONTROL, and CLOCK INHIBIT should not be changed when the CLOCK is high. Data is synchronously shifted one stage left or one stage right depending on the state of the LEFT/RIGHT CONTROL, with the positive CLOCK edge. Data clocked into the first of 32 register states is available at the SHIFT LEFT or SHIFT RIGHT OUTPUT respectively, on the next negative CLOCK transition (see Data Transfer Table). No shifting occurs on the positive CLOCK edge if the CLOCK INHIBIT line is at a high level. With the RECIRCULATE CONTROL low, data in the 32nd stage is shifted into the first stage when the LEFT/RIGHT CONTROL is low and from the 1st stage to the 32nd stage when the LEFT/RIGHT CONTROL is high.

PIN CONNECTION



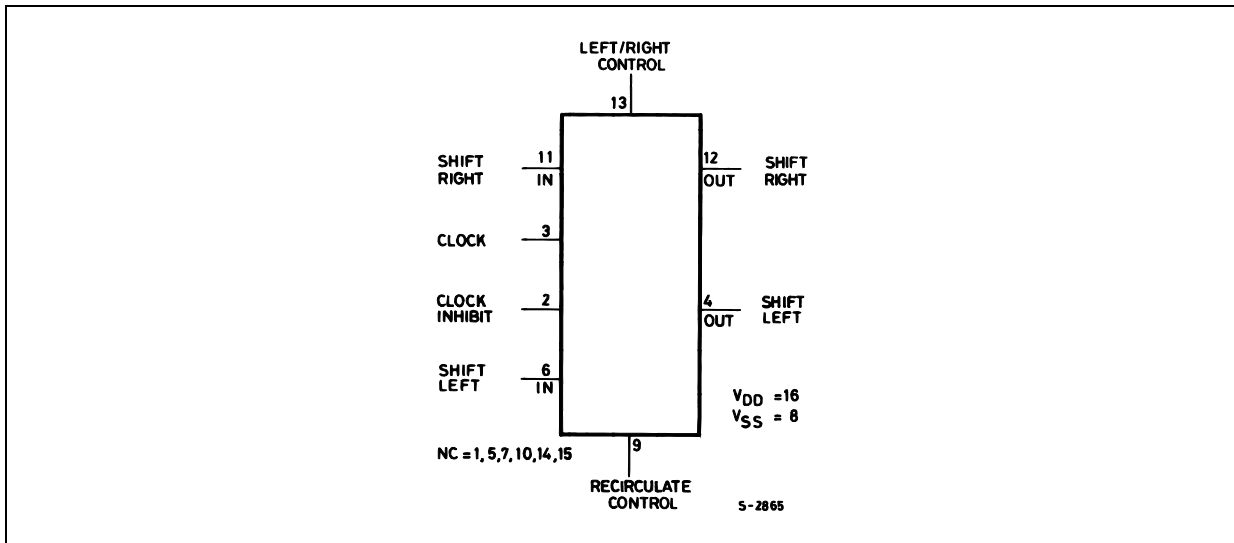
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
11	SHIFT RIGHT IN	Shift Right In
6	SHIFT LEFT IN	Shift Left In
12	SHIFT RIGHT OUT	Shift Right Out
4	SHIFT LEFT OUT	Shift Left Out
3	CLOCK	Clock
2	CLOCK INHIBIT	Clock Inhibit
13	LEFT/RIGHT CONTROL	Left/Right Control
9	RECIRCULATE CONTROL	Recirculate Control
1, 5, 7, 10, 14, 15	NC	Not Connected
8	V _{SS}	Negative Supply Voltage
16	V _{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM







TRUTH TABLES

CONTROL

Left/Right Control	Clock Inhibit	Recirculate Control	Action	Input Bit Origin
H	L	H	Shift Left	Shift Left Input
H	L	L	Shift Left	Stage 1
L	L	H	Shift Right	Shift Right Input
L	L	L	Shift Right	Stage 32
X	H	X	No Shift	-

DATA TRANSFER

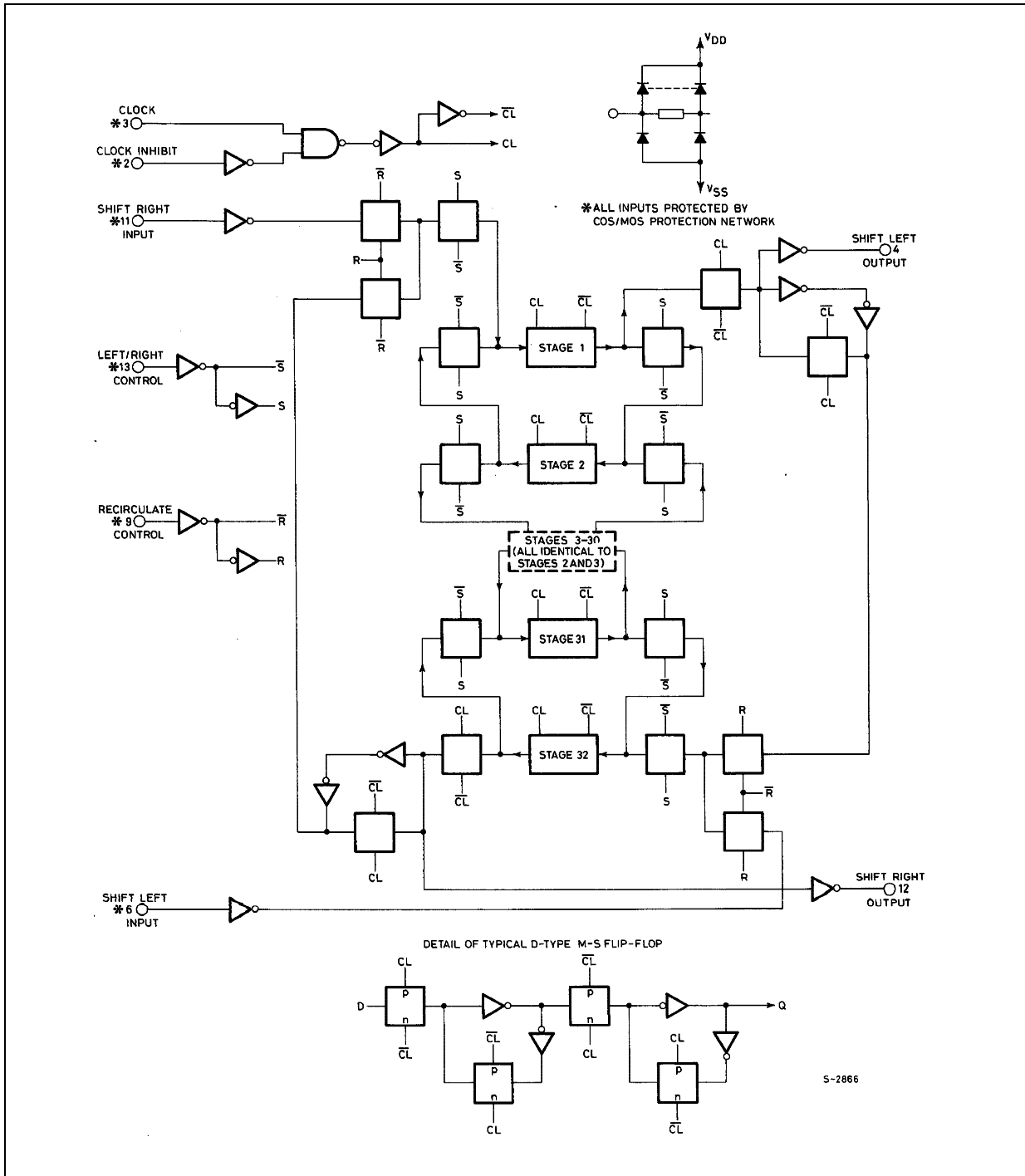
INITIAL STATE			CLOCK	Resulting State	
Data Input	Clock Inhibit	Internal Stage	Level Change	Internal Stage Q	Output
L	L	X		L	NC
X	L	L		NC	L
H	L	X		H	NC
X	L	H		NC	H
X	H	H	X	NC	NC

X : Don't Care

NC : No Change

For Shift-Right Mode: Data Input = SHIFT RIGHT INPUT (Pin 11); Internal Stage = Stage1 (Q1); Output = SHIFT LEFT OUTPUT (Pin 4).
 For Shift-Left Mode: Data Input = SHIFT LEFT INPUT (Pin 6); Internal Stage = Stage32 (Q32); Output = SHIFT RIGHT OUTPUT (Pin 12).

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V _I (V)	V _O (V)	I _{ol} (μ A)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I _L	Quiescent Current	0/5			5		0.04	5		150		150	μ A
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V _{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I _{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	± 0.1		± 1		± 1	μ A
C _I	Input Capacitance		Any Input				5	7.5					pF

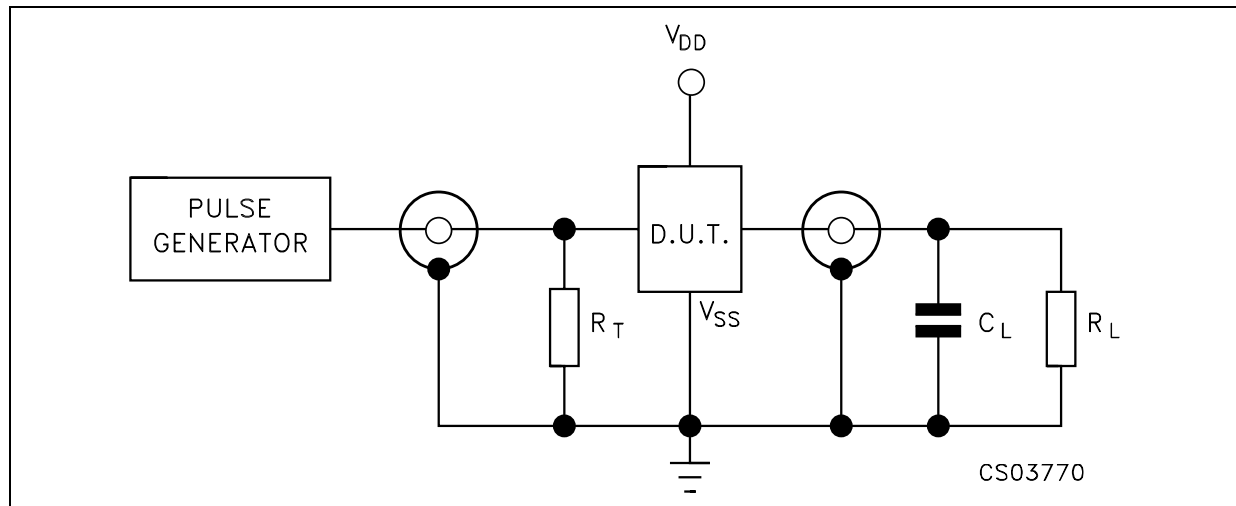
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{K}\Omega$, $t_r = t_f = 20\text{ ns}$)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time	5			360	720	ns
		10			165	330	
		15			115	230	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{setup}	Data Setup Time	5		100	50		ns
		10		20	10		
		15		10	5		
t_{hold}	Data Hold Time	5		275	170		ns
		10		100	75		
		15		75	50		
t_W	Clock Input Pulse Width Low Level	5		450	225		ns
		10		230	115		
		15		190	95		
t_W	Clock Input Pulse Width High Level	5		280	140		ns
		10		150	75		
		15		140	70		
f_{CL}	Maximum Clock Input Frequency	5		1	2		MHz
		10		2.5	5		
		15		3	6		

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

TEST CIRCUIT



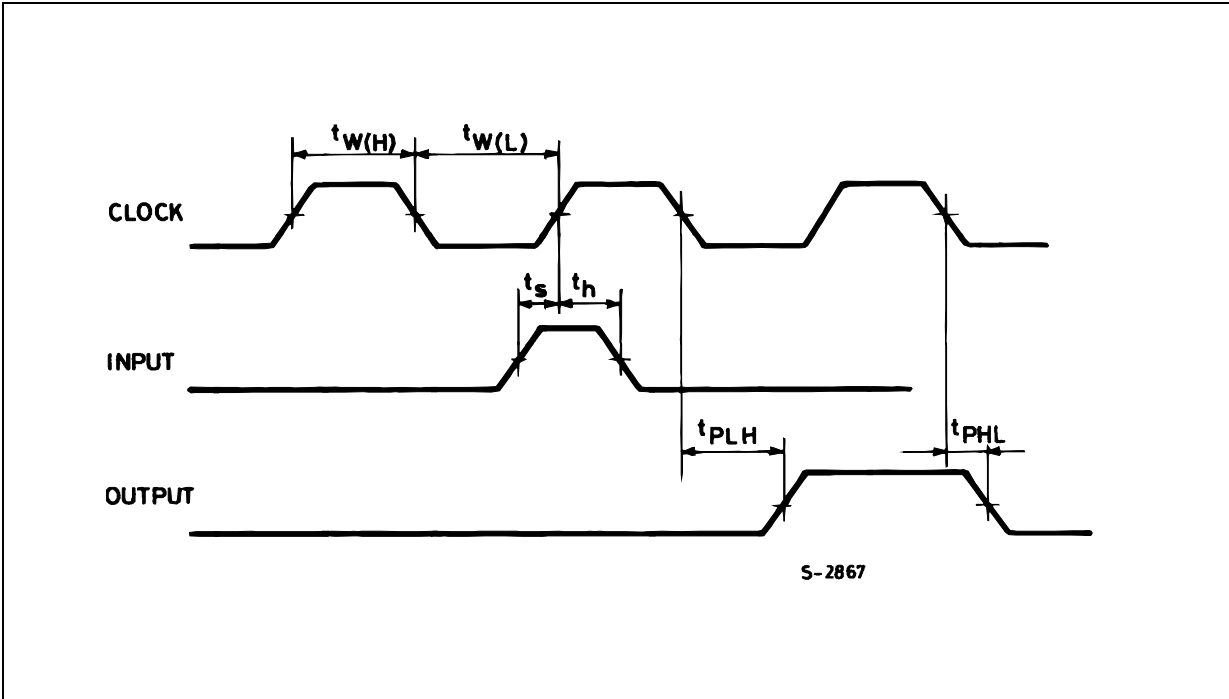
$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)

$R_L = 200\text{K}\Omega$

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

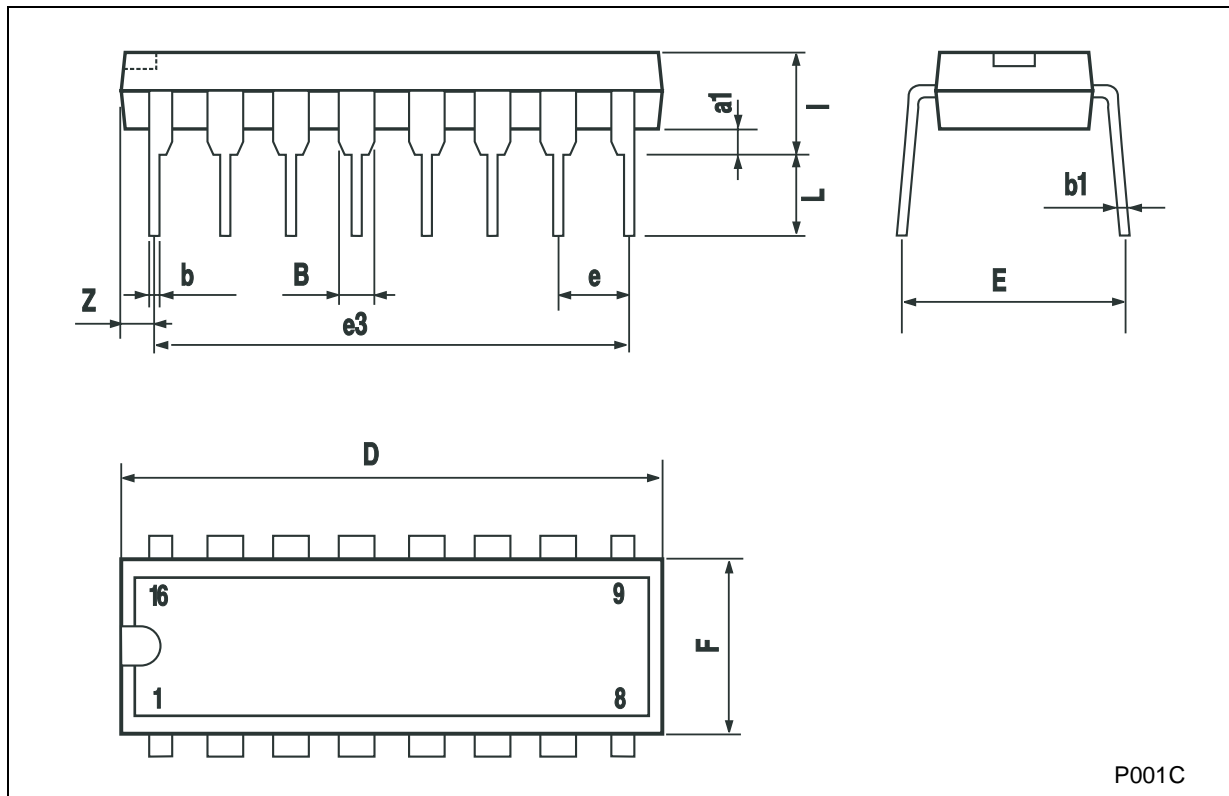
HCF40100B

WAVEFORM : PROPAGATION DELAY, DATA SETUP, TIME, CLOCK PULSE WIDTH (f=1MHz; 50% duty cycle)



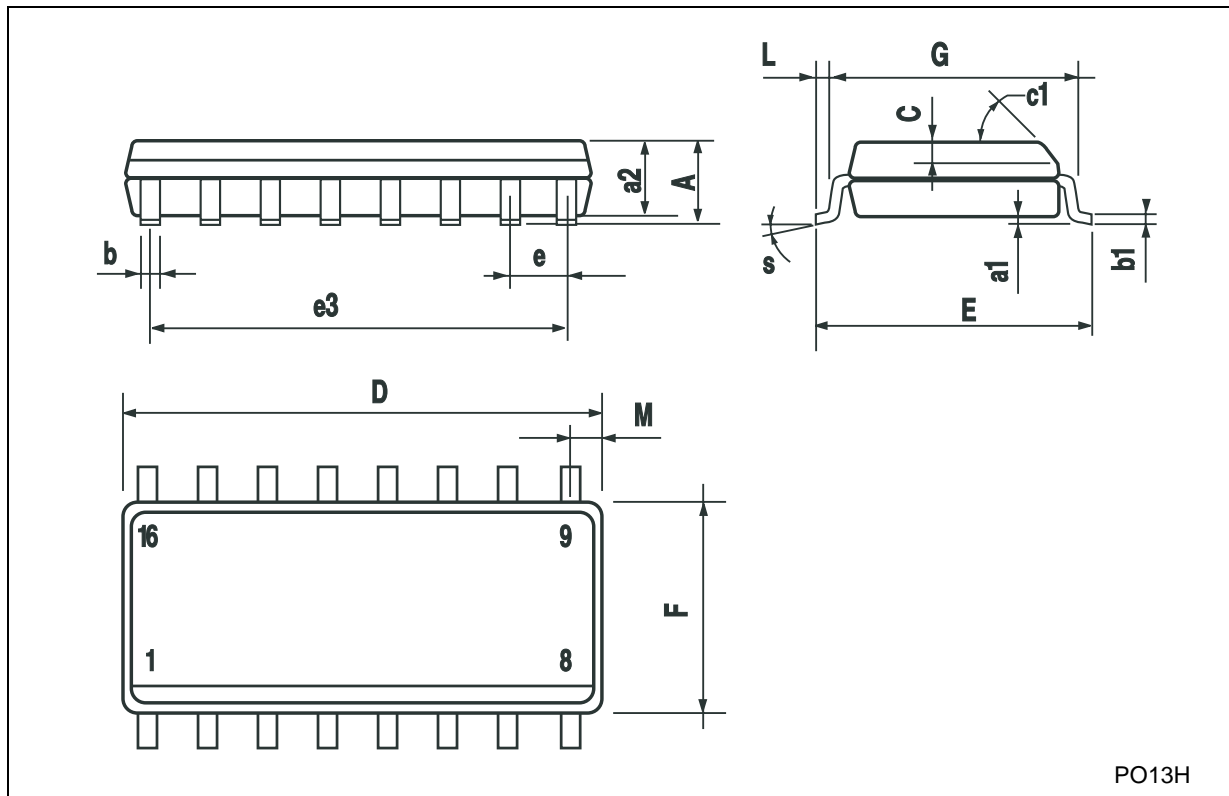
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

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