MOTOROLA

# MC145146

## 4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

The MC145146 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

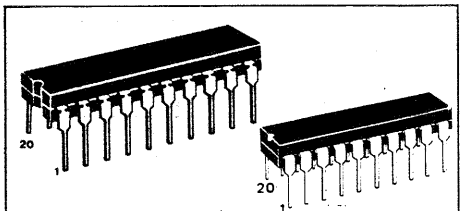
The MC145146 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, 12-bit programmable reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit divide-by-A counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145146 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and the MC145146

- General Purpose Applications
  - CATV
  - AM/FM Radios
  - Two Way Radios
  - TV Tuning
  - Scanning Receivers
  - Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @5 Vdc
- Programmable Reference Divider for Values Between 3 and 4095
- On- or Off-Chip Reference Oscillator Operation
- Dual Modulus 4-Bit Data Bus Programming
- ÷N Range=3 to1023, ÷A Range= 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options —
  Single Ended (Three State)
  Double Ended

## CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

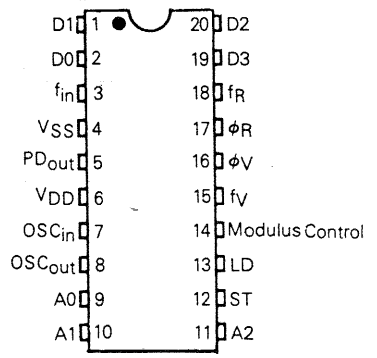
4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

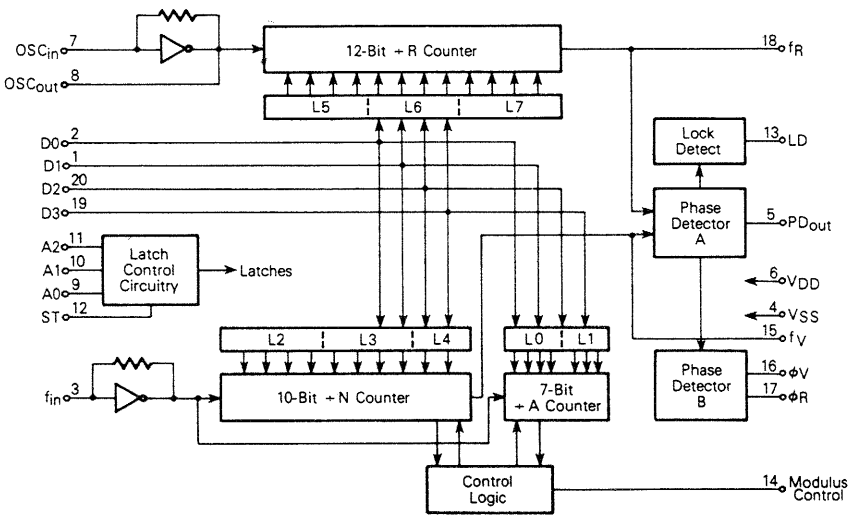



L SUFFIX
CERAMIC PACKAGE
CASE 732

P SUFFIX
PLASTIC PACKAGE
CASE 738

PIN ASSIGNMENT




ADI-837

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | −0.5 to +10 | Vdc |
| Input Voltage, All Inputs | $V_{in}$ | −0.5 to $V_{DD}$+0.5 | Vdc |
| DC Current Drain Per Pin | I | 10 | mA |
| DC Current Drain $V_{DD}$ or $V_{SS}$ Pins | I | 30 | mA |
| Operating Temperature Range | $T_A$ | −40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS**

| Characteristic | Symbol | $V_{DD}$ | $T_{low}$ | | 25°C | | | $T_{high}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| Power Supply Voltage Range | $V_{DD}$ | – | 3 | 9 | 3 | – | 9 | 3 | 9 | Vdc |
| Output Voltage 0 Level $V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 3 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| | | 5 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| | | 9 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| $V_{in}$ = or $V_{DD}$ 1 Level | $V_{OH}$ | 3 | 2.95 | – | 2.95 | 3 | – | 2.95 | – | |
| | | 5 | 4.95 | – | 4.95 | 5 | – | 4.95 | – | |
| | | 9 | 8.95 | – | 8.95 | 9 | – | 8.95 | – | |
| Input Voltage 0 Level $V_O$ = 2.5 or 0.5 | $V_{IL}$ | 3 | – | 0.9 | – | 1.35 | 0.9 | – | 0.9 | Vdc |
| $V_O$ = 4.5 or 0.5 | | 5 | – | 1.5 | – | 2.75 | 1.5 | – | 1.5 | |
| $V_O$ = 8.5 or 1.5 | | 9 | – | 2.7 | – | 4.05 | 2.7 | – | 2.7 | |
| $V_O$ = 0.5 or 2.5 1 Level | $V_{IH}$ | 3 | 2.10 | – | 2.10 | 1.65 | – | 2.10 | – | |
| $V_O$ = 0.5 or 4.5 | | 5 | 3.5 | – | 3.5 | 2.75 | – | 3.5 | – | |
| $V_O$ = 1.5 or 8.5 | | 9 | 6.3 | – | 6.3 | 4.95 | – | 6.3 | – | |
| Output Current Source $V_{OH}$ = 2.7 | $I_{OH}$ | 3 | −0.44 | – | −0.35 | −0.66 | – | −0.22 | – | mAdc |
| $V_{OH}$ = 4.6 | | 5 | −0.64 | – | −0.51 | −0.88 | – | −0.36 | – | |
| $V_{OH}$ = 8.5 | | 9 | −1.3 | – | −1.0 | −1.3 | – | −0.7 | – | |
| $V_{OL}$ = 0.3 Sink | $I_{OL}$ | 3 | 0.44 | – | 0.35 | 0.66 | – | 0.22 | – | |
| $V_{OL}$ = 0.4 | | 5 | 0.65 | – | 0.51 | 0.88 | – | 0.36 | – | |
| $V_{OL}$ = 0.5 | | 9 | 1.3 | – | 1.0 | 1.3 | – | 0.7 | – | |
| Output Current Modulus Control Source $V_{OH}$ = 2.7 | $I_{OH}$ | 3 | 0.15 | – | 0.25 | 0.5 | – | 0.08 | – | mAdc |
| $V_{OH}$ = 4.6 | | 5 | 0.45 | – | 0.75 | 1.5 | – | 0.23 | – | |
| $V_{OH}$ = 8.5 | | 9 | 0.75 | – | 1.25 | 2.5 | – | 0.38 | – | |
| $V_{OL}$ = 0.3 Sink | $I_{OL}$ | 3 | 0.48 | – | 0.8 | 1.6 | – | 0.24 | – | mA |
| $V_{OL}$ = 0.4 | | 5 | 0.90 | – | 1.5 | 3 | – | 0.45 | – | |
| $V_{OL}$ = 0.5 | | 9 | 2.10 | – | 3.5 | 7 | – | 1.05 | – | |
| Input Current Other Inputs | $I_{IL}$ | 9 | – | ±0.3 | – | ±00001 | ±0.1 | – | ±1.0 | μAdc |
| $f_{in}$, $OSC_{in}$ | | 9 | – | ±15 | – | ±5 | ±10 | – | ±8 | |
| $f_{in}$, $OSC_{in}$ | $I_{IH}$ | 9 | – | ±15 | – | ±5 | ±10 | – | ±8 | |
| Other Inputs | | 9 | – | ±0.3 | – | ±0.00001 | ±0.1 | – | ±1.0 | |
| Input Capacitance | $C_{in}$ | 3-9 | – | 10 | – | 6 | 10 | – | 10 | pF |
| Output Capacitance | $C_{out}$ | 3-9 | – | 10 | – | 6 | 10 | – | 10 | pF |
| Quiescent Current | $I_{DD}$ | 3 | – | 800 | – | 200 | 800 | – | 1600 | μAdc |
| | | 5 | – | 1200 | – | 300 | 1200 | – | 2400 | |
| | | 9 | – | 1600 | – | 400 | 1600 | – | 3200 | |
| 3-State Leakage Current $PD_{out}$ | $I_{IL}$ | 9 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±3.0 | μAdc |

NOTE: $T_{low}$ = −40°C
$T_{high}$ = 85°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$).

## SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

| Characteristic | Symbol | $V_{DD}$ | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Output Rise Time | $t_{TLH}$ | 3 | – | 100 | 200 | ns |
| | | 5 | – | 50 | 100 | |
| | | 9 | – | 40 | 80 | |
| Output Fall Time | $t_{THL}$ | 3 | – | 100 | 200 | ns |
| | | 5 | – | 50 | 100 | |
| | | 9 | – | 40 | 60 | |
| Propagation Delay Time<br>Clock to Modulus Control | $t_{PLH}$ | 3 | – | 80 | 160 | ns |
| | | 5 | – | 50 | 100 | |
| | | 9 | – | 30 | 60 | |
| | $T_{PHL}$ | 3 | – | 80 | 160 | ns |
| | | 5 | – | 50 | 100 | |
| | | 9 | – | 30 | 60 | |
| Setup Times<br>Data to ST | $t_{su}$ | 3 | 10 | 0 | – | ns |
| | | 5 | 10 | 0 | – | |
| | | 9 | 10 | 0 | – | |
| Address to ST | $t_{su}$ | 3 | 80 | 60 | – | ns |
| | | 5 | 50 | 30 | – | |
| | | 9 | 30 | 18 | – | |
| Hold Time<br>Data, Address to ST | $t_h$ | 3 | 35 | 15 | – | ns |
| | | 5 | 25 | 10 | – | |
| | | 9 | 20 | 10 | – | |
| Output Pulse Width<br>$\phi_R$, $\phi_V$ with $f_R$ in<br>Phase with $f_V$ | $t_{WH(\phi)}$ | 3 | 70 | 120 | 170 | ns |
| | | 5 | 50 | 100 | 150 | |
| | | 9 | 30 | 80 | 130 | |
| Input Rise and Fall Times<br>$OSC_{in}$, $f_{in}$ | $t_{TLH}$<br>$t_{THL}$ | 3 | – | – | 5 | µs |
| | | 5 | – | – | 4 | |
| | | 9 | – | – | 2 | |
| Input Pulse Width<br>$OSC_{in}$, $f_{in}$, Strobe | $t_W$ | 3 | 40 | 30 | – | ns |
| | | 5 | 35 | 20 | – | |
| | | 9 | 25 | 15 | – | |

## FREQUENCY CHARACTERISTICS

| Characteristic | | Symbol | $V_{DD}$ | $T_{low}$ | | 25°C | | | $T_{high}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Typ | Max | Min | Max | |
| Operating Frequency<br>$OSC_{in}$ | Input = SQ Wave $V_{DD} - V_{SS}$ | $f_{max}$ | 3 | – | 17 | – | 27 | 14 | – | 12 | MHz |
| | | | 5 | – | 33 | – | 55 | 27 | – | 21 | |
| | | | 9 | – | 35 | – | 65 | 35 | – | 33 | |
| | Input = Sin Wave 500 mV ptp | $f_{max}$ | 3 | – | 11 | – | 21 | 10 | – | 9 | MHz |
| | | | 5 | – | 20 | – | 34 | 17 | – | 15 | |
| | | | 9 | – | 17 | – | 34 | 17 | – | 15 | |
| Operating Frequency<br>$f_{in}$ | Input = SQ Wave $V_{DD} - V_{SS}$ | $f_{max}$ | 3 | – | 9 | – | 15 | 8 | – | 7 | MHz |
| | | | 5 | – | 19 | – | 30 | 15 | – | 15 | |
| | | | 9 | – | 31 | – | 52 | 26 | – | 22 | |
| | Input = Sin Wave 500 mV ptp | $f_{max}$ | 3 | – | 10 | – | 15 | 7 | – | 6 | MHz |
| | | | 5 | – | 18 | – | 31 | 15 | – | 15 | |
| | | | 9 | – | 21 | – | 31 | 15 | – | 15 | |

$T_{low} = -40°C$
$T_{high} = 85°C$

**DATA INPUTS (Pins 2, 1, 20, 19)** – Information at these inputs is transferred to the internal latches when the ST input is in the high state. Pin 19 (D3) is most significant.

**$f_{in}$ (Pin 3)** – Input to ÷N portion of synthesizer. $f_{in}$ is typically derived from loop VCO and is AC coupled into Pin 3. For larger amplitude signals (standard CMOS-logic levels), DC coupling may be used.

**$V_{SS}$ (Pin 4)** – Circuit Ground.

**$PD_{out}$ (Pin 5)** – Three-state output of phase detector for use as loop error signal.

Frequency $f_V > f_R$ or $f_V$ Leading: Negative Pulses.
Frequency $f_V < f_R$ or $f_V$ Lagging: Positive Pulses.
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State.

**$V_{DD}$ (Pin 6)** – Positive power supply.

**$OSC_{in}$, $OSC_{out}$ (Pins 7 and 8)** – These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from $OSC_{in}$ to ground and $OSC_{out}$ to ground. $OSC_{in}$ may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to $OSC_{in}$, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to $OSC_{out}$.

**ADDRESS INPUTS (Pins 9, 10, 11)** – A0, A1 and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

| A2 | A1 | A0 | Selected | Function | D0 | D1 | D2 | D3 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Latch 0 | ÷A Bits | 0 | 1 | 2 | 3 |
| 0 | 0 | 1 | Latch 1 | ÷A Bits | 4 | 5 | 6 | – |
| 0 | 1 | 0 | Latch 2 | ÷N Bits | 0 | 1 | 2 | 3 |
| 0 | 1 | 1 | Latch 3 | ÷N Bits | 4 | 5 | 6 | 7 |
| 1 | 0 | 0 | Latch 4 | ÷N Bits | 8 | 9 | – | – |
| 1 | 0 | 1 | Latch 5 | Reference Bits | 0 | 1 | 2 | 3 |
| 1 | 1 | 0 | Latch 6 | Reference Bits | 4 | 5 | 6 | 7 |
| 1 | 1 | 1 | Latch 7 | Reference Bits | 8 | 9 | 10 | 11 |

**ST (Pin 12)** – When high, this input will enter the data that appears at the D0, D1, D2 and D3 inputs, and when low, will latch that information. When high, any changes in the data information will be transferred into the latches.

**LD (Pin 13)** – Lock detector signal. High level when loop is locked ($f_R$, $f_V$ of same phase and frequency). Pulses low when loop is out of lock.

**MODULUS CONTROL (Pin 14)** – Signal generated by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷N counter has counted the rest of the way down from its programmed value (N-A additional counts since both ÷N and ÷A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value ($N_T = N \cdot P + A$ where P and P+1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the ÷N counter and A the number programmed into the ÷A counter.

**$f_V$ (Pin 15)** – This is the output of the ÷N counter that is internally connected to the phase detector input. With this output available, the ÷N counter can be used independently.

**$\phi V$, $\phi R$ (Pins 16 and 17)** – These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see $PD_{out}$).

If frequency $f_V$ is greater than $f_R$ or if the phase of $f_V$ is leading, then error information is provided by $\phi V$ pulsing low. $\phi R$ remains essentially high.

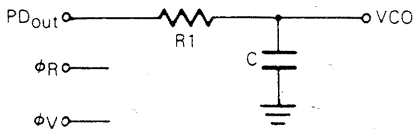
If the frquency $f_V$ is less than $f_R$ or if the phase of $f_V$ is lagging, then error information is provided by $\phi R$ pulsing low. $\phi V$ remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both $\phi V$ and $\phi R$ remain high except for a small minimum time period when both pulse low in phase.

**$f_R$ (Pin 18)** – This is the output of the ÷R counter that is internally connected to the phase detector input. With this output available, the ÷R counter can be used independently.

## PHASE LOCKED LOOP — LOW PASS FILTER DESIGN

A)

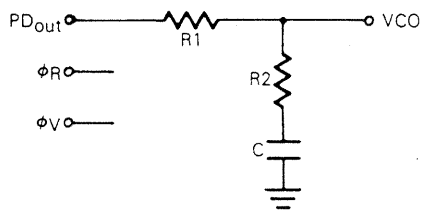



$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NR1C}}$$

$$\zeta = 0.5\omega_N (N/K_\phi K_{VCO})$$

$$F(s) = \frac{1}{R1CS + 1}$$

B)

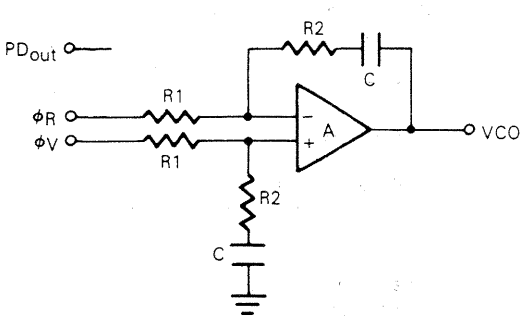



$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NC(R1 + R2)}}$$

$$\zeta = 0.5\omega_N (R2C + N/K_\phi K_{VCO})$$

$$F(s) = \frac{R2CS + 1}{S(R1C + R2C) + 1}$$

C)




$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NCR1}}$$

$$\zeta = \frac{\omega_N R2C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R2CS + 1}{R1CS}$$

NOTE: Sometimes R1 is split into two series resistors each R1 ÷ 2. A capacitor $C_C$ is then placed from the midpoint to ground to further filter $\phi_V$ and $\phi_R$. The value for $C_C$ should be such that the corner frequency of this network does not significantly affect $\omega_N$.

DEFINITIONS: N = Total Division Ratio in feedback loop

$K_\phi = V_{DD}/4\pi$ for $PD_{out}$

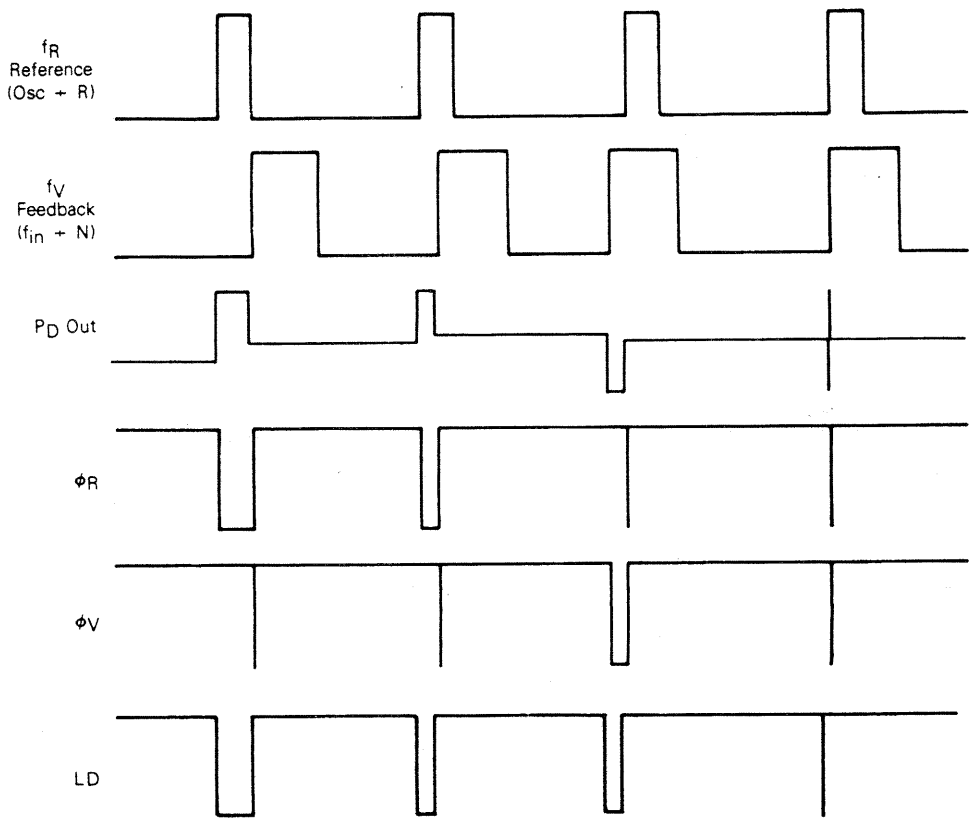
$K_\phi = V_{DD}/2\pi$ for $\phi_V$ and $\phi_R$

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

for a typical design $\omega_N \cong (2\pi/10)\, f_r$ (at phase detector input)

$\zeta \cong 1$

FIGURE 1
PHASE DETECTOR OUTPUT WAVEFORMS




NOTE: The $P_D$ output state is equal to either $V_{DD}$ or $V_{SS}$ when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

RELATED PHASE LOCKED LOOP FREQUENCY SYNTHESIZERS

| Part Number | Format | Prescale | Phase Detector |
|---|---|---|---|
| MC145144 | 4-Bit Data | Single Modulus | 3 State |
| MC145145 | Bus Input | Single Modulus | 3 State/2 Output |
| MC145146 | Format | Dual Modulus | 3 State/2 Output |
| MC145151 | Parallel Input | Single Modulus | 3 State/2 Output |
| MC145152 | Format | Dual Modulus | 2 Output |
| MC145155 | Serial Input | Single Modulus | 3 State/2 Output |
| MC145156 | Format | Dual Modulus | 3 State/2 Output |
| MC145157 | | Single Modulus | 3 State/2 Output |
| MC145158 | | Dual Modulus | 3 State/2 Output |
| MC145159 | | Dual Modulus | 3 State/Analog |

FIGURE 2
TYPICAL $f_{in}$ MAXIMUM FREQUENCY vs $V_{DD}$
INPUT = 500 mV ptp

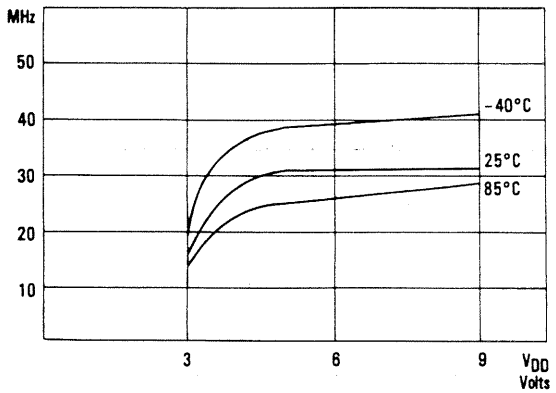



FIGURE 3
TYPICAL $OSC_{in}$ MAXIMUM FREQUENCY vs $V_{DD}$
INPUT = 500 mV ptp

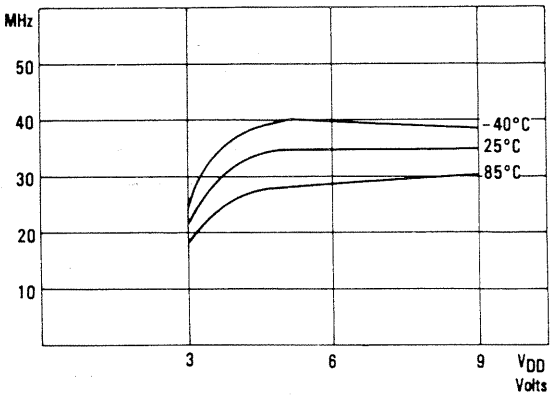



FIGURE 4
TYPICAL $f_{in}$ MAXIMUM FREQUENCY vs $V_{DD}$
INPUT = SQ WAVE ($V_{DD} - V_{SS}$)

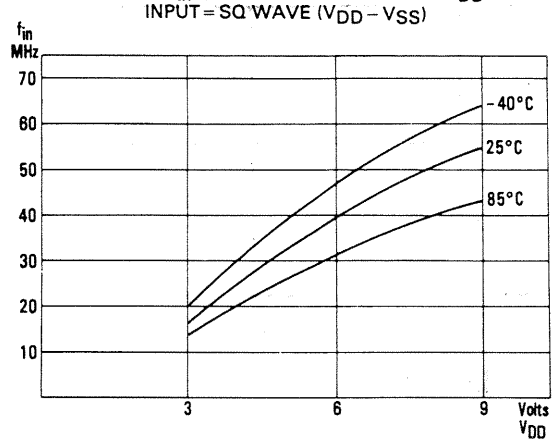



FIGURE 5
TYPICAL $OSC_{in}$ MAXIMUM FREQUENCY vs $V_{DD}$
INPUT = SQ WAVE ($V_{DD} - V_{SS}$)

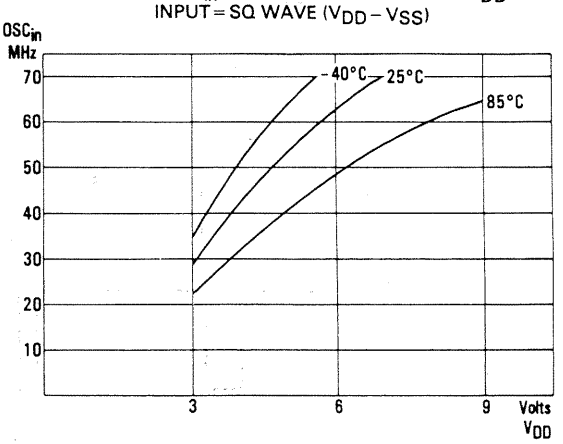
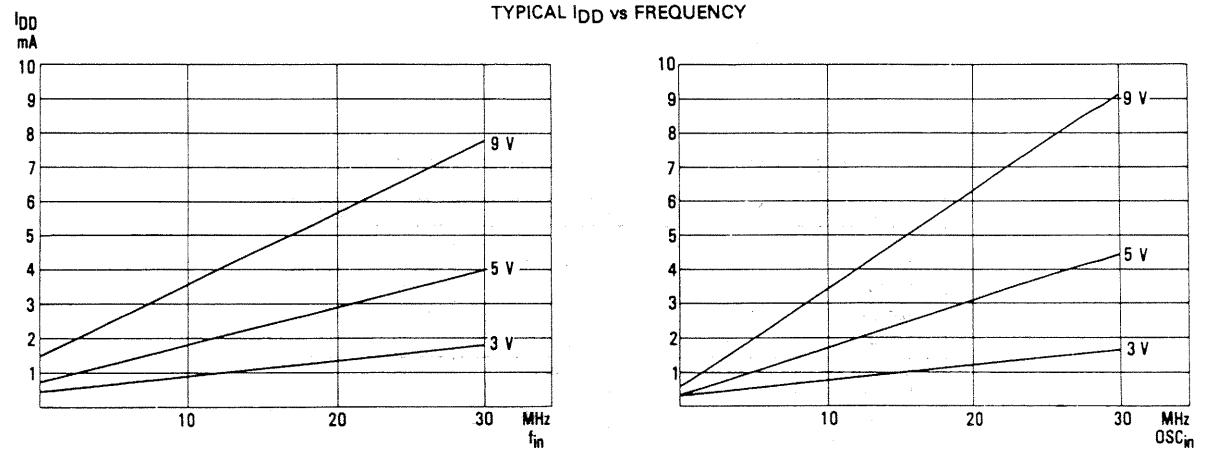



FIGURE 6
TYPICAL $I_{DD}$ vs FREQUENCY



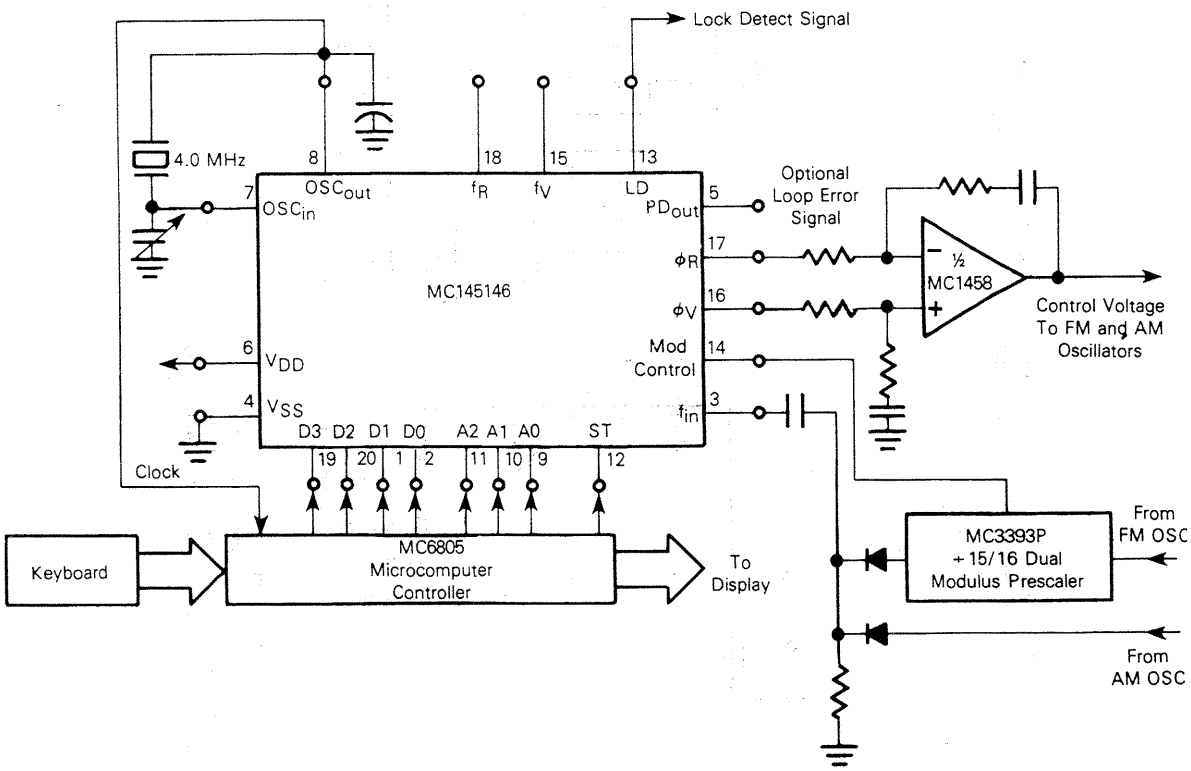

NOTE: To compute total $I_{DD}$ add component due to $f_{in}$ with that due to $OSC_{in}$.

## APPLICATIONS

The features of the MC145146 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor controlled system this strobe input is accessed when the phase lock loop is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

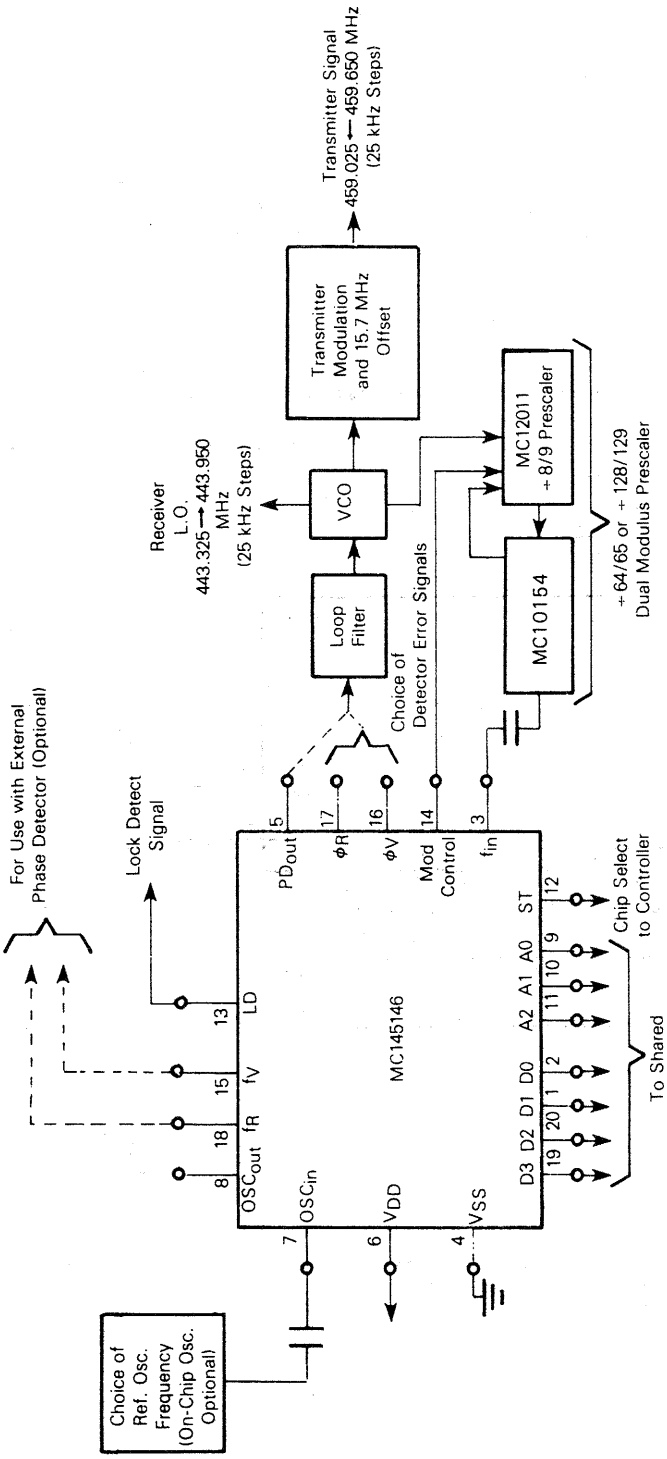
The device architecture allows the user to establish any integer reference divide value between 3 and4096. The wide selection of ÷ R values permits a high degree of flexibility in choosing the reference oscillator frequency. As a result the reference oscillator can frequently be chosen to serve multiple system functions such as a second local oscillator in a receiver design or a microprocessor system clock. Typical applications that takes advantage of these MC145146 features including the dual modulus capability are shown in Figures 7, 8 and 9.

FIGURE 7 — FM/AM BROADCAST RADIO SYNTHESIZER



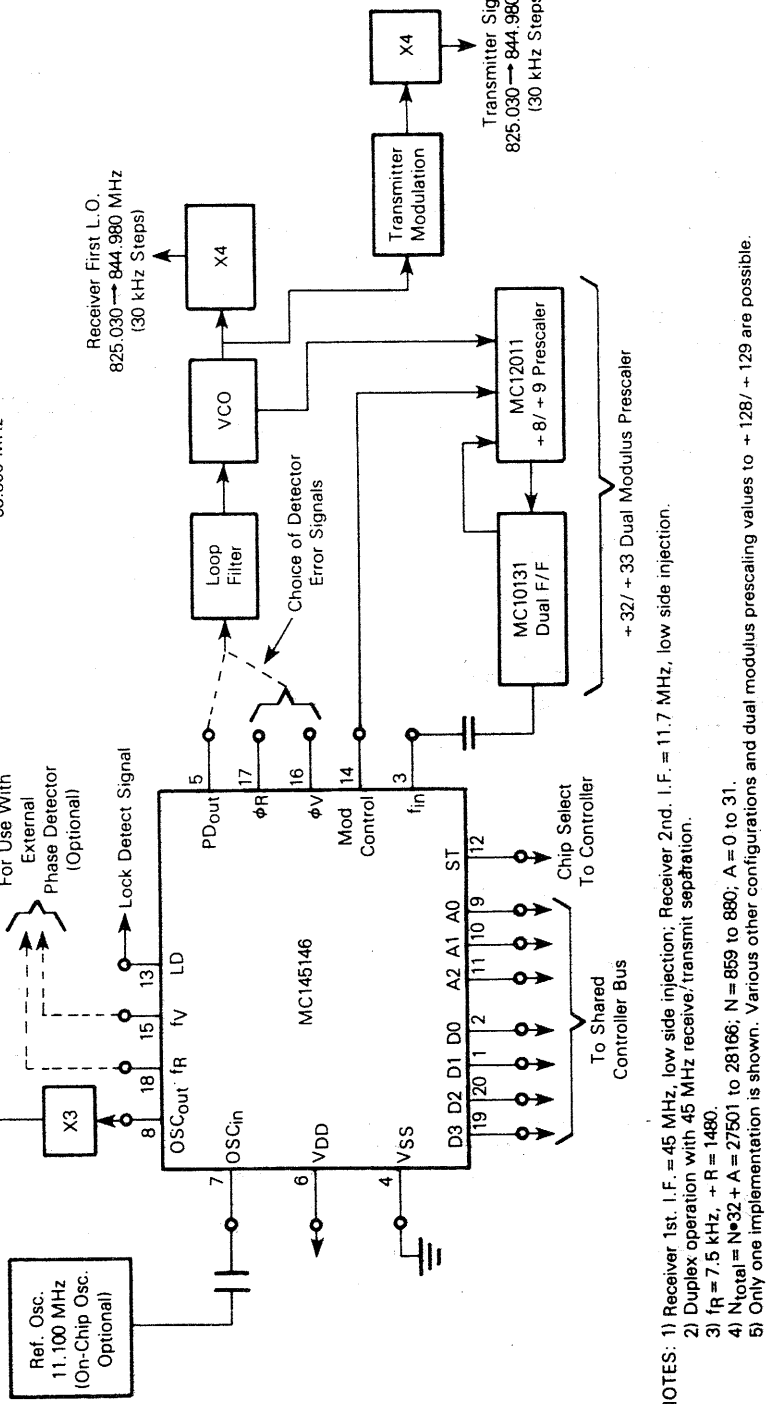

NOTES: 1) For FM: Channel spacing = $f_R$ = 25 kHz, ÷ R = 160.
For AM: Channel spacing = $f_R$ = 1 kHz, ÷ R = 4000.
2) Various channel spacings and reference oscillator frequencies can be chosen since any ÷ R value from 3 to 4096 can be established.
3) Data and address lines are inactive and high impedance when pin 12 is low. Their interface with the controller may therefore be shared with other system functions if desired.

FIGURE 8 — SYNTHESIZER FOR UHF MOBILE RADIO TELEPHONE CHANNELS DEMONSTRATES USE OF THE MC145146 IN MICROPROCESSOR/MICROCOMPUTER CONTROLLED SYSTEMS OPERATING TO SEVERAL HUNDRED MHz




NOTES: 1) Receiver I.F. = 10.7 MHz, low side injection.
2) Duplex operation with 5 MHz receive/transmit separation.
3) $f_R$ = 25 kHz, + R chosen to correspond with desired reference oscillator frequency.
4) $N_{total}$ = 17733 to 17758 = N•P + A; N = 277, A = 5 to 30 for P = 64.

FIGURE 9 — 666 CHANNEL, COMPUTER CONTROLLED, MOBILE RADIO TELEPHONE SYNTHESIZER FOR 800 MHz CELLULAR RADIO SYSTEMS




NOTES: 1) Receiver 1st. I.F. = 45 MHz, low side injection; Receiver 2nd. I.F. = 11.7 MHz, low side injection.
2) Duplex operation with 45 MHz receive/transmit separation.
3) $f_R$ = 7.5 kHz, ÷ R = 1480.
4) Ntotal = N•32 + A = 27501 to 28166; N = 859 to 880; A = 0 to 31.
5) Only one implementation is shown. Various other configurations and dual modulus prescaling values to ÷ 128/ ÷ 129 are possible.