Low Cost Monolithic Sample-Hold SHM-LM-2

FEATURES

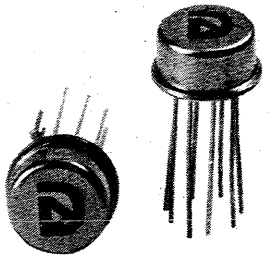
- 5 μsec. Acquisition Time
- .01% Gain Accuracy
- TTL/CMOS Logic Compatible
- ±5V to ±18V Supplies
- TO-99 Package
- Low Cost

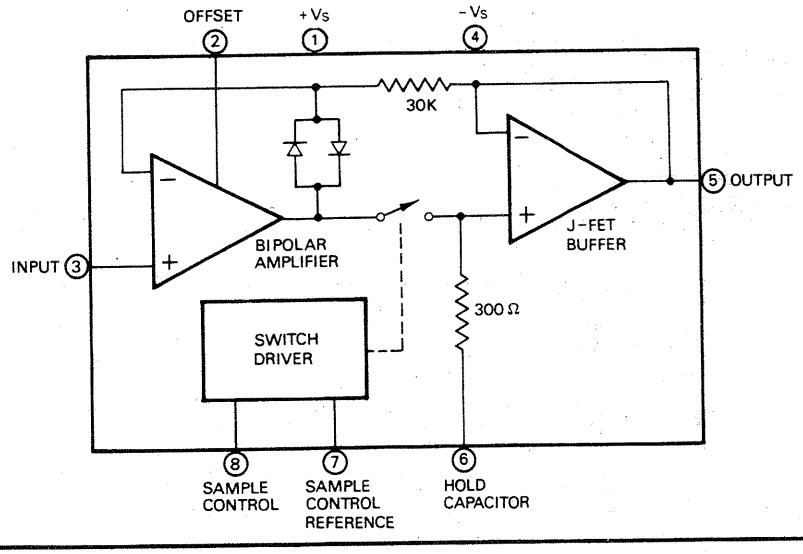
GENERAL DESCRIPTION

The SHM-LM-2 is a low cost monolithic sample-hold circuit with excellent performance features. It is self-contained requiring only an external hold capacitor with the value selected by the user for desired speed and accuracy characteristics. Acquisition time is 6 μsec. for a 10V change to .01% using a 1000pF capacitor and 25 μsec. using a .01 μF capacitor. It is 5 μsec. and 20 μsec. respectively for a 10V change to 0.1%. This device is internally configured as a unity gain follower with a gain error of less than .01% in the sample mode.

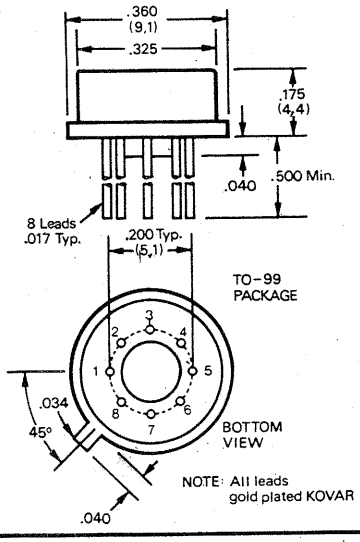
The circuit consists of a bipolar input amplifier, a low leakage electronic switch, and an FET output amplifier. The monolithic fabrication process combines P channel junction FET's with bipolar transistors to achieve a low noise, high input impedance output amplifier. Other important specifications include 10^{10} ohms input impedance and 1 MHz bandwidth. Aperture time is less than 100 nsec. and hold mode feedthrough is less than .005%. Hold mode droop is 200 μV/msec. max. with a 1000pF hold capacitor and 20 μV/msec. max. with a .01 μF capacitor. The SHM-LM-2 can operate over a power supply range of ±5V to ±18V.

Applications include sampling for A/D conversion, deglitching circuits, automatic zeroing circuits, and analog demultiplexing circuits. It is recommended that the holding capacitor (C_H) be a teflon, polystyrene, or polypropylene type for best results. Operating temperature range is 0°C to 70°C for SHM-LM-2 and -55°C to +125°C for SHM-LM-2M.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+POWER SUPPLY
2	OFFSET ADJUST
3	INPUT
4	−POWER SUPPLY
5	OUTPUT
6	HOLD CAPACITOR (C_H)
7	SAMPLE CONTROL REF.
8	SAMPLE CONTROL

DATEL-INTERSIL, INC. 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 95134

SPECIFICATIONS
(Typical at 25°C, ±15V supplies and C_H = .01 μF unless otherwise stated)

MAXIMUM RATINGS

Power Supply Voltage, pins 1 & 4	±18V
Input Voltage, pin 3	±Supply
Sample Control to Sample Reference, pin 8 to pin 7	+7, -30V
Hold Capacitor Short Circuit	10 sec.

INPUTS

Input Voltage Range	±11.5V min.
Input Overvoltage, no damage	± Supply
Input Impedance	10^{10} ohms
Input Bias Current	10 nA typ., 50 nA max.
Sample Control	TTL or CMOS
Sample Control Input Current[1]	10 μA max.

OUTPUT

Output Voltage Range	±11.5V min.
Output Current, S.C. protected	±5 mA
Output Impedance	0.5 ohm

PERFORMANCE

Gain	+1.000, +0, −.01%
Output Offset Voltage, adj. to zero	±7 mV max.
Offset Voltage Drift, SHM-LM-2	20 μV/°C
Offset Voltage Drift, SHM-LM-2M	10 μV/°C[2]
Sample to Hold Offset	2.5 mV max.
Hold Mode Feedthrough	.01% max.
Power Supply Rejection Ratio	80 dB min.
Output Noise, hold mode (10Hz-100kHz)	8.5 μV RMS
Hold Mode Droop, C_H = 1000 pF	200 μV/msec. max.
C_H = .01 μF	20 μV/msec. max.

DYNAMIC RESPONSE

Acquisition Time	
10V Change, C_H = 1000 pF	5 μsec. to 0.1%
10V Change, C_H = 1000 pF	6 μsec. to .01%
20V Change, C_H = 1000 pF	7 μsec. to 0.1%
20V Change, C_H = 1000 pF	8 μsec. to .01%
10V Change, C_H = .01 μF	20 μsec. to 0.1%
10V Change, C_H = .01 μF	25 μsec. to .01%
Aperture Delay Time	100 nsec.
Hold Mode Settling Time[3]	800 nsec.
Bandwidth, Sample Mode, −3 dB	1 MHz

POWER REQUIREMENT

Voltage, rated performance	±15VDC
Voltage Range, operating	±5V to ±18VDC
Quiescent Current	6 mA

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range, SHM-LM-2	0°C to +70°C
SMM-LM-2M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Case	8 pin TO-99

NOTES:
1. For either Sample Control or Sample Control Reference inputs
2. 28 μV/°C max.
3. The time for the output to settle within 1 mV of final value after the logic command to switch into hold mode.

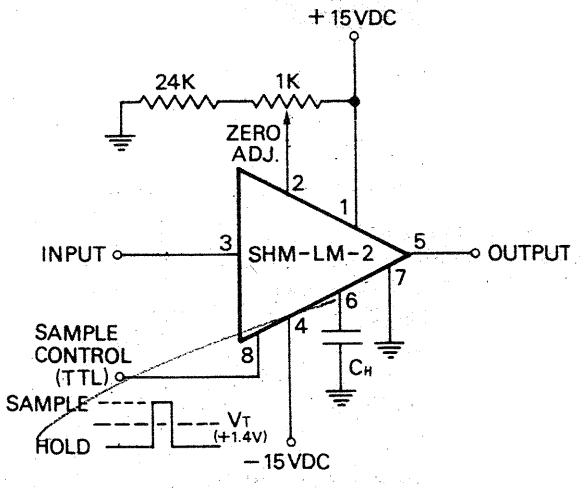
ORDERING INFORMATION

Model	Operating Temp. Range
SHM-LM-2	0°C to 70°C
SHM-LM-2M	-55°C to +125°C

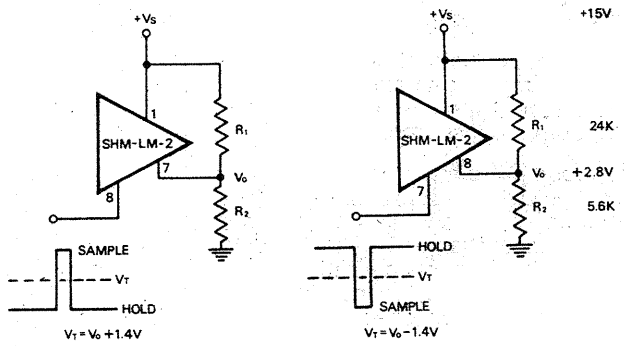
Trimming Potentiometer, TP1K

THE SHM-LM-2 IS COVERED BY GSA CONTRACT

CONNECTION DIAGRAM



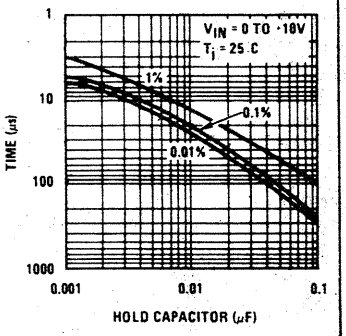
SAMPLE-CONTROL CONNECTIONS



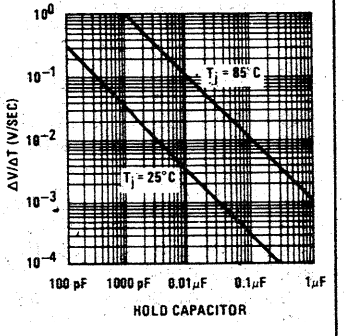
For TTL connect pin 7 to ground.

For TTL use values shown on right.

ACQUISITION TIME



HOLD MODE DROOP



TECHNICAL NOTES

1. The sample to hold offset can be adversely affected by stray capacitive coupling from input sample control signals to the hold capacitor. It is recommended that a guard ring connected to the output be put around pin 6 in a circuit board layout in order to minimize this effect.
2. For various types of logic inputs the logic threshold (V_T) is set by two biasing resistors as shown in the diagram. Inverted or non-inverted pulses may be used by using either pin 7 or pin 8 as the sample control input.